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Design And Analysis Of One-Lane Traffic Controller

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Abstract :

In this work the designe and time anylises of an adaptive signal controller to coordinate traffic signals at two ende of one-lane road to support two-way traffic is obtaind by using Complex Programmable Logic Device (CPLD) . A sensor will be positioned at each end of the road to detect cars entering and leaving the road. Time will be allocated to traffic in each direction according to traffic flow measurment obtained from the sensors during each 5-minutes period. An XC9500XL CPLDs is used to implement the design schematiclly by using Xillinx ISE Design suite 13.2.

Key words: Traffic Signal Controller, Schematic Design,CPLD XC9500XL, Xillinx ISE .

تصميم و تحليل لمسيطر مرور ذات ممر باتجاه واحد

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الخلاصة :

في هذا العمل تم أعداد التصميم الرقمي والتحليل الزمني لمسيطر متكيف على حركة المرور في مسار مروري ذات أتجاه وبنهايتيين واحد وذلك بأستخدام برنامج تصميمي تحليلي (Xillinx ISE Design suite 13.2) . يتم التحسس بمرور العربه في المسار من خلال متحسسات توضع فيبداية و نهاية المسار للتحسس بخروج ودخول العربه للمسار. التنظيم الزمني للمسيطر تم أعتمادا على حالة المتحسسات لكل 5 دقائق . لقد تم بناء التصميم الرقمي للمسيطر بأسلوب الهيكله البرمجيه بأستخدام الرقاقه (XC9500XL CPLDs) .

1. Introduction

In many places,two-way automobile must be supported by a single lane road, such as on narrow bridges in the country, roads under repair, and other narrow streets, as shown in **Figure(1)**, the single lane usually connects normal two-lane road segments.The control of the two-way traffic in this singl lane requires special traffic signals at each end of the single lane road that allow traffic to flow in the other direction, alternating back and forth.

For each direction change, the traffic signal controller must halt traffic in one direction and wait until the lane is clear before allowing traffic to proceed in the opposite direction .To achieve optimum traffic, the period of time allocated to traffic in each direction should be adjusted according to the traffic conditions, with the direction corresponding to heavier traffic allocated a longer period of time than the other. Traffic flow measurments can be made by using sensors embedded in the road at each end of the lan [1,2,3]

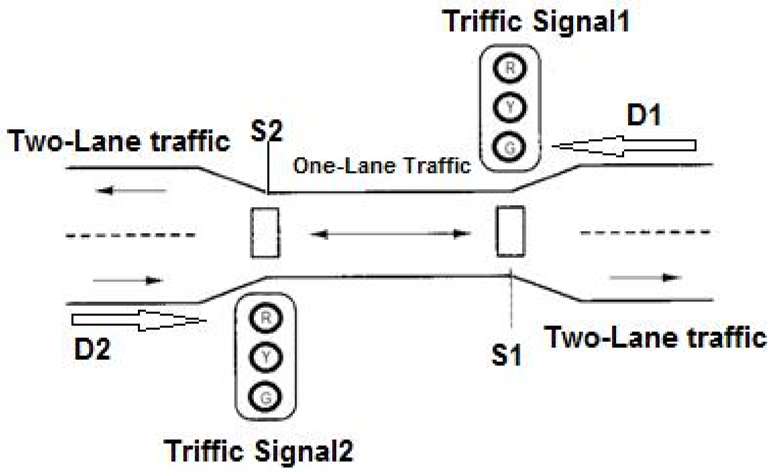


Fig .(1) Two-Way Traffic on a One-Lane Road

2. System Requirements

The traffic controller will control the red, yellow, and green lamps of two traffic signals (G1, Y1, and R1) for signal 1 and (G2, Y2, and R2) for signal 2, one at each end of the road as shown in **Figure(1**).

It is assumed that each of the six lights has a separate ON/OFF control line. Inputs to the traffic controller include signals from two sensors, S1 and S2, placed at each end of the road. Each sensor generates a pulse whenever crossed by a car. A manual RESET button will also be provided to initialize the controller. The primary function of the controller is to determine when to switch the traffic lights from one color to the next.

For cars moving in **direction1**, G1 will be ON for a time T1, which will be recomputed every 5 minutes (choose) according to the traffic flow in each direction. After time T1, the yellow light Y1 will be turned ON for a single time unit Ty (10 seconds will be used as the basic time unit), after which red light R1 will be turned ON until the controller is ready to activate G1 again.

For cars moving in **direction 2**, light G2 will not be turned ON until after the last car moving in direction1 has left the road. The number of cars still on the road can be determined by comparing the number of cars entering the road, as signaled by one sensor, to the number of cars leaving the road, as signaled by the other sensor.

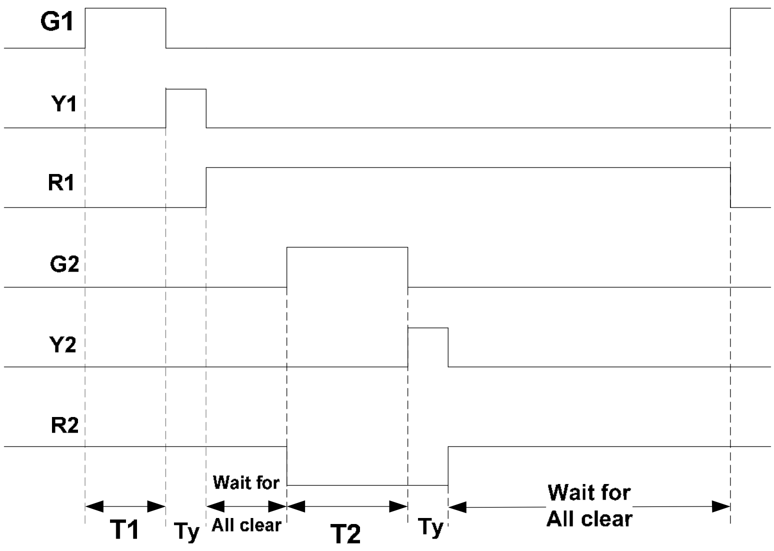


Fig .(2) Traffic Controller Timing Diagram

When the difference between these counts is zero, it will be assumed that the road is clear. The duration of green light G2, T2 will be computed as

T2= Ttot- T1 **(1)**

Where Ttot is a total amount of green-light time.

Ttot will be split between directions 1 and direction 2 according to the relative traffic flow in each direction, this timing pattern is illustrated in **Fig.2**

The primary components of the controller include a time-base generator. a counter to determine whether cars remain on the road. A traffic counter to measure relative traffic flow in the two directions, a circuit to compute the green light time allocations for the two directions, and a state machine control unit, **Fig.3** presents a block diagram of the traffic light controller.[4,5,6]

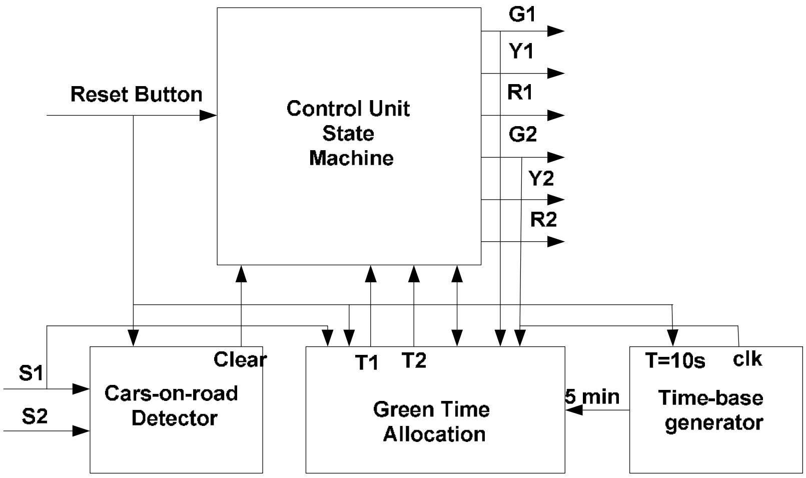


Fig .(3) Traffic controller block diagram

2.1 Times-Base Generator

The time-base generator will generate a clock signal that will be used to compute the times at which lights will he switched. The 10-second yellow light period will be assumed to be the shortest event; all other switching times will be computed as multiple of 10 seconds. Thus, a clock signal with a period of 10 seconds will be used. The amount of green light time allocated to each direction will be recomputed every 5 minutes. Therefore, the clock signal will increment a counter that will be used to generate a pulse every 5 minutes [4]

2.1.1 Logic Design of Time-Base Generator.

A clock signal with a period of 10 seconds will provide the time base for the controller. This clock signal will be generated by a test bench wave form program, a short pulse at the end of every 5-minute period is required to signal that it is time to sample the traffic counter and recomputed the green time allocations. This pulse will be derived by a simple binary counter incremented by the clock generator.

Since 5 min = 5 x 60 s = 30 x 10 s,

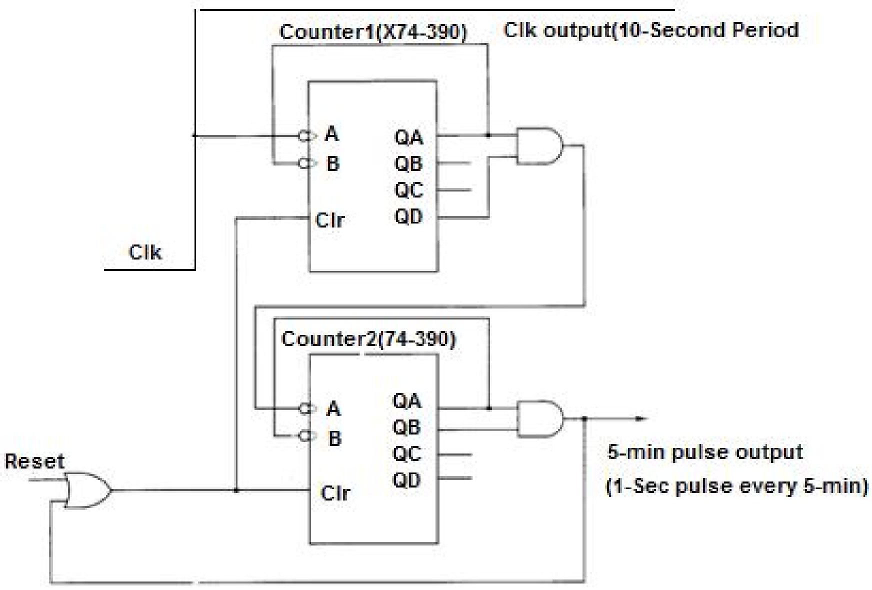
A X74_390 is a dual, 4-bit decade asynchronous 30 module counter can be used for this purpose, as shown in **Figure (4.a)**

Counter1 is incremented once every 10 seconds and counter2 is incremented when counter1 changes from 9→0.

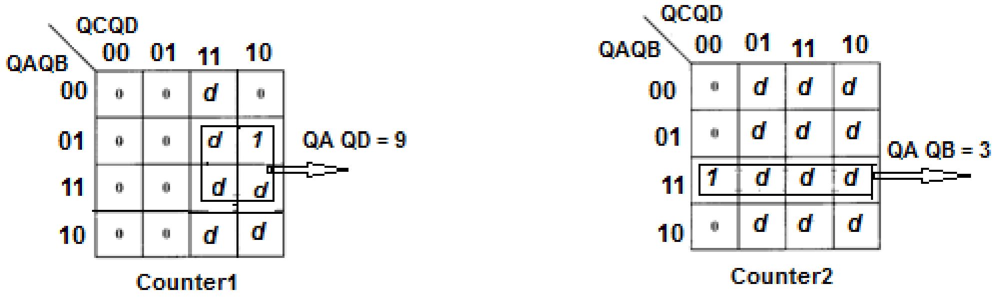
Referring to the K-map in **Figure (4.b)** and realizing that counter1 will never exceed 9, counter2 should be incremented for the condition $\mathbf{Q_A.Q_D = 1}$.

Likewise, counter2 will never exceed a count of 3, therefore, from the K-map in **Fig.4.c** both counters should be reset for the counter2 condition $\mathbf{Q_A.A_B = 1}$.

In addition, both counters are also reset by the master RESET signal. The complete time-base generator circuit is shown in **Figure (4.a)** [5,6,7]



(a)



(b) **(c)**

Fig .(4) time base generator circuit design (a) logic diagram (b) counter1 = 9 (c) counter 2 = 3

2.2 Cars-on-Road Counter

To determine whether cars remain on the road prior to activating a green light, a counter will be used to compute the difference between the numbers of cars entering the road, NE and the number of cars leaving the road, NL. The road is assumed to be all clear whenever

NE - NL = 0 **(2)**

The number of cars entering the road is determined by counting pulses from one sensor, and the number of cars leaving is determined by counting pulses from the other sensor. Since the only condition of interest is whether **NE - NL = 0**.

The actual counts are not needed. Therefore, an up/down counter will be used that will be incremented by pulses from sensor S1 and decremented by pulses from sensor S2, counter output signal will indicate the condition **NE - NL = 0**.as shown in **Figure (5)**

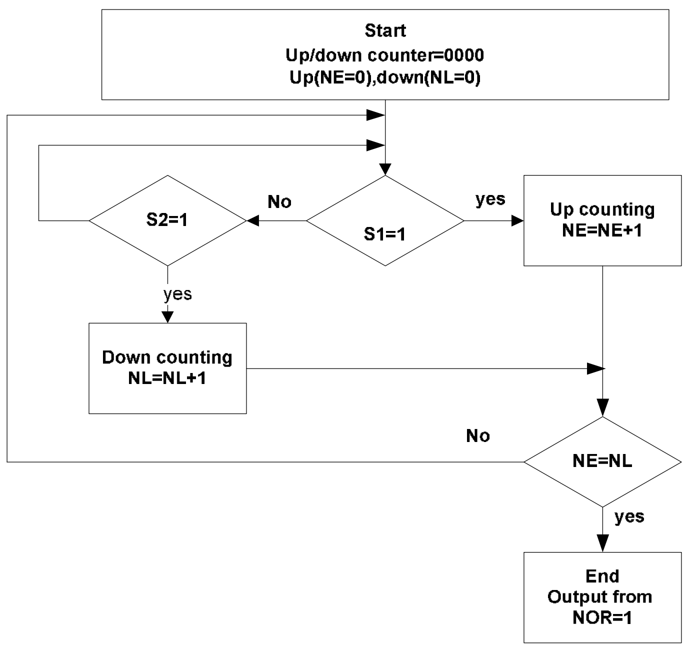


Fig .(5) flow chart for the cars on road counting

2.2.1 Logic Design of Cars-on-Road Counter.

the road will be considered clear whenever the number of cars that leave the road, NL is equal to the number of cars that enter the road, NE To detect this condition, a binary up/down counter will be used as follows. Pulses from sensors S1 and S2 will be generated each time a car enters or leaves the road.

For traffic in **direction1**, pulses from S1 indicate cars entering the road, while for direction 2 they indicate cars leaving the road and vice versa for sensor S2 Since only the difference between cars entering and leaving is significant, pulses from S1 will be used to increment the counter, and pulses from S2 will decrement the counter. Any time the count is zero, the counter will have been incremented and decremented an equal number of times; that is, **NL - NE = 0**, signaling that the road is clear.

The binary up/down counter used for this module must have a sufficient number of bits to count the largest number of cars that can enter the road without having left, that is, to compute the largest expected value of **NL – NE**, assumed that a 4-bit binary counter is sufficient, that is, that no more than 15 cars (choose) will ever be on the road at any one time.

The **CB4X2** is a 4-bit binary up/down counter with separate clock inputs for counting up and down. It will be configured as shown in **Figure (6)**, with the UP clock input controlled by pulses from sensor S1 and the DOWN clock input controlled by S2 a 4-input NOR gate detects a count of zero by producing an output of logic 1, indicating that **NE = NL** thus indicating that all cars that entered the road have left.[7,8,9]

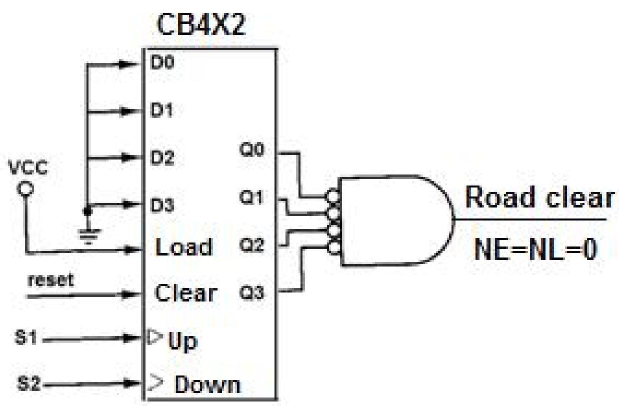


Fig .(6) digital design of car on road counters circuit

2.3 Traffic Counter.

To determine the relative amount of green light time allocated to each direction, a counter will be used to compute the difference between the numbers of cars traversing the road in each direction. As shown in **Figure (7)**.

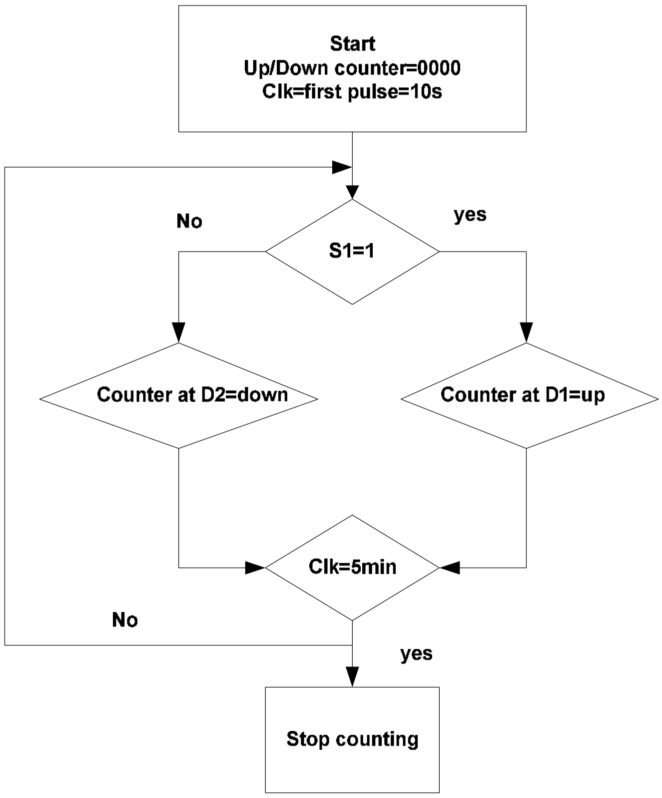


Fig .(7) flow chart for the traffic counting

As with the cars-on-road counter, the traffic counter will be incremented by cars moving in one direction and decremented by cars moving in the opposite direction. Pulses from S1 will be used in both cases. The count will be sampled every 5 minutes. Signaled by a pulse from the clock (time base generator), after which the counter will be reset to zero to begin the next 5-minutes period.

2.3.1 Logic Design of Traffic Counter.

The operation of the traffic counter is similar to that of the cars-on-road counter is measured the difference between the numbers of cars traversing the road in each direction. An up/down counter can again be used. Incremented by cars moving in one direction and decremented by cars moving in the opposite direction, only pulses from one sensor S1 will be used with a signal from the control unit indicating the traffic direction.

To minimize complexity, it will be assumed that the difference between the numbers of cars traversing the road in the two directions will be no more than 15, so an 1-bit counter will be sufficient. Again the **CB4X2** 4-bit binary up/down counter will be used. As shown in **Figure (8)**. It will be incremented for each pulse on S1 while G1 is active and decremented for each pulse on S1 while G2 is active. The counter will be reset every 5 minutes.[8,9]

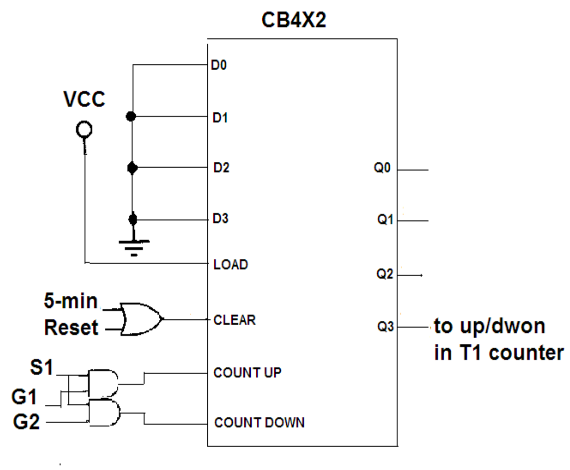


Fig .(8) digital design of Triffic counter circuits

2.4 Green Time Allocation.

This module will recomputed the green light durations T1 and T2 at the end of each 5-minutes period based on the output of the traffic counter. Assuming:

***D1** to be the traffic count in direction1.*

***D2** to be the traffic count in direction2.*

***T1** will be increased if **D1- D2** > **0** and decreased if **D1- D2** < **0**.*

***T2** will be computed as **Ttot - T1**.*

*Limit values will be used to ensure that neither T1 nor T2 drop below a minimum period of 40 seconds to prevent stalling traffic flow in either direction as shown in **Figure (9)**.*

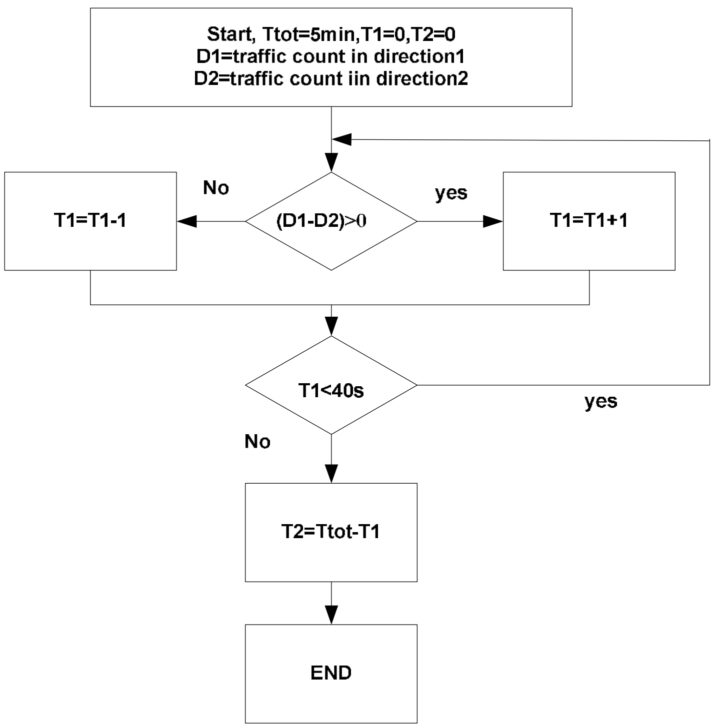


Fig .(9) flow chart for the green time duration counting

2.4.1 Logic Design of Green Time Allocation.

The total amount of time allocated to green lights in one complete traffic cycle is

Ttot = T1 + T2 **(3)**

Where T1 is the amount of time allocated to green light G1 in direction1

T2 the amount of time for light G2 in direction 2

If the traffic over as-minute period is greater in direction1 than in direction2, T1, will be increased by one time unit and T2 reduced by one time unit, keeping Ttot constant.

To prevent traffic from being stalled in either direction, neither time will be reduced below a specified minimum value.

We assign **Ttot = 160 s**, which corresponds to **16** periods of clock signal CLK.

This time will be split between T1 and T2, The circuit is shown in **Figure (10)**.

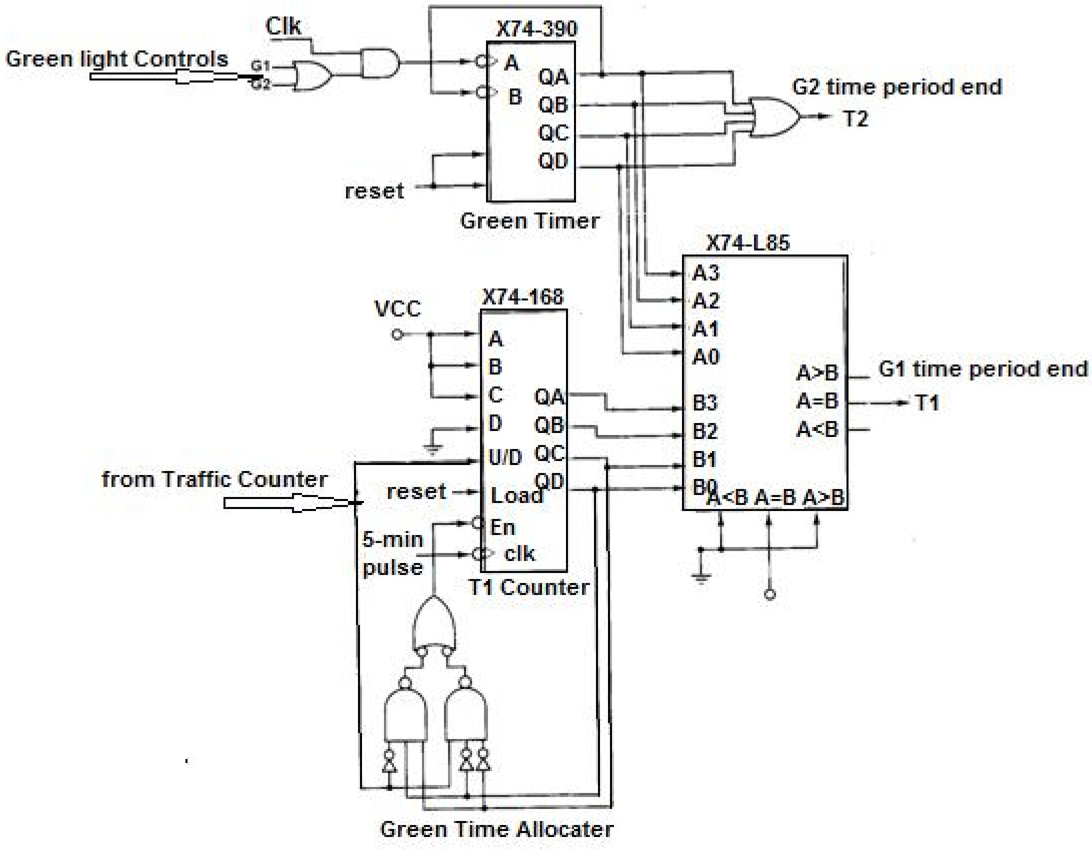


Fig .(10) Digital design of Green timer circuit

The **X74-390** green timer counter is incremented every 10 seconds while either light is green. That is, while G1 = 1 or G2 = 1. The clock signal is disabled when G1= G2 = 0.

G1 is assumed to be turned on at a count of 0. A **X74L85** comparator will detect the condition t = T1, at which time G1 will be turned off and the counter will be stopped until G2 turns on. Then it will count to 15 **($Q_DQ_CQ_BQ_A$) = 1111**, at which time T2, will be set to 1 to make the control unit turn off G2.

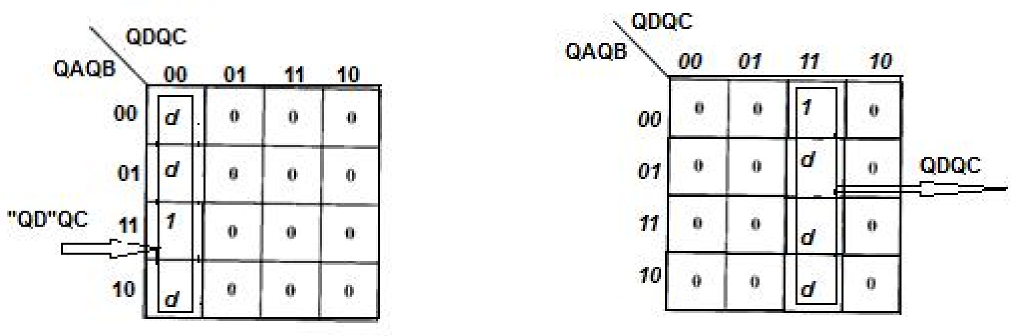
The allocation of time for T1 will be determined by a second counter. This counter will be initialized to a value of 7 at reset time, setting **T1 = T2 = 80s**.

The counter will then incremented or decremented after each 5-minutes time period, according time of **40 seconds** will be used for T1 and T2, Therefore, the counter will not be decremented if **T1 = 3** and will not incremented if **T1 = 12**. The conditions for inhibiting the decrementing and incrementing of the counter are derived from the K-maps of **Fig.11**.

Note that both maps contain don't-care conditions since the count will never be allowed to go below 3 or above 12. The logic expression used to inhibit the counter is the following:

$$\mathbf{INHIBIT = DN \cdot (\overline{Q}_D\, \overline{Q}_C) + \overline{DN} \cdot (Q_D .\, Q_C)} \qquad (4)$$

Where DN is the signal from the traffic counter controlling the UP/DN input of the T1 counter, The **INHIBIT** signal is applied to the **EN** input of the T1 counter, disabling the counter when **INHIBIT = 1** and enabling the counter when **INHIBIT = 0**,



(a) **(b)**

Fig .(11) K-maps for logic to enforce green time limits (a) inhibit down count K-map (b) Inhibit up count K-map

2.5 State Machine Control Unit.

The state machine control unit will coordinate the operation of the traffic light controller and generate the ON/OFF signals for the six lamps, cycling through them according to the timing diagram in **Figure (2)**.

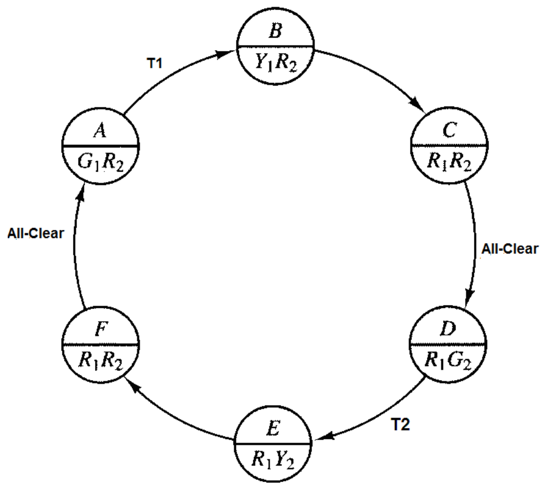


Fig .(12) state machine diagram for the one-lane Traffic light controller

*with switching times based on the outputs of the cars-on-road detector and the green time allocation module as shown in **Figure (12)**.*[5,9,10]

2.5.1 Logic Design of Control Unit.

*The control unit requires six states, corresponding to the times during which the light is green and yellow in each direction and during which both lights are red. The timing states were shown in **Table (1)**. The six states are defined as flow:*

Table .(1) the six states

State	*Light1*	*Light2*
A	*G1*	*R2*
B	*Y1*	*R2*
C	*R1*	*R2*
D	*R1*	*G2*
E	*R1*	*Y2*
F	*R1*	*R2*

Note that the control unit leaves states A and D after times T1 and T2.

Respectively, as defined previously, states B and E is each exited after a single clock period. States C and F are exited as soon as the number of cars exiting the road is equal to the number of cars that entered the road, that is, as soon as the output of the cars-on-road counter is zero, signaling the all-clear condition.

In this state machine, the state transitions occur in a fixed sequence, as in a simple module-6 counter; that is, the simply cycles through states A-B-C-D-E-F-A, and so on. The times of the state changes depend on the three inputs T1, T2, and All clear.

To design this state machine we design a module-6 counter with decoder to derive the six outputs. The counter would be incremented for each state change. Alternatively, a state machine design can be developed from a state table of six rows and eight columns, corresponding to the six states and three inputs.

This implementation would require three flip-flops and assorted combinational logic. Use a one-hot state assignment, and realize the state machine with a 6-bit shift register, as shown in **Fig.13**. Each shift register output corresponds to one state of the machine.

Outputs A and B control lights G1 and Y1, respectively, while outputs D and E control lights G2 and Y2. Light R1 is on whenever G1 and Y1 are both off, and likewise R2 is on whenever G2 and Y2 are both off. These output conditions are the following:

$$G1 = Q_A,\ G2 = Q_D,\ Y1 = Q_B,\ Y2 = Q_E,\ R1 = (\overline{G1 + Y1}),\ R2 = (\overline{G2 + Y2}) \qquad (5)$$

When the RESET button is pressed, bit 0 of the shift register will be initialized to 1 and the other bits to 0 to start the machine in state A. The shift enable input will then be activated and the register shifted one time for each condition indicated in the state diagram. These conditions are combined into the following shift-enable signal:

$$\mathbf{SHIFT\_EN = (A \cdot T1) + B + (C.\ CLR) + (D.\ T2) + E + (F.\ CLR)} \qquad \mathbf{(6)}$$

As shown in **Figure (13)**, the SHIFT_EN signal is ANDed with CLK to drive the two Shift Registers **(SR4RLE),** SR1-CK1 inputs, which provides the clock signal during shift operations. CLK also drives SR2- CK2 inputs, which clocks the register during load operations.[1,7,10]

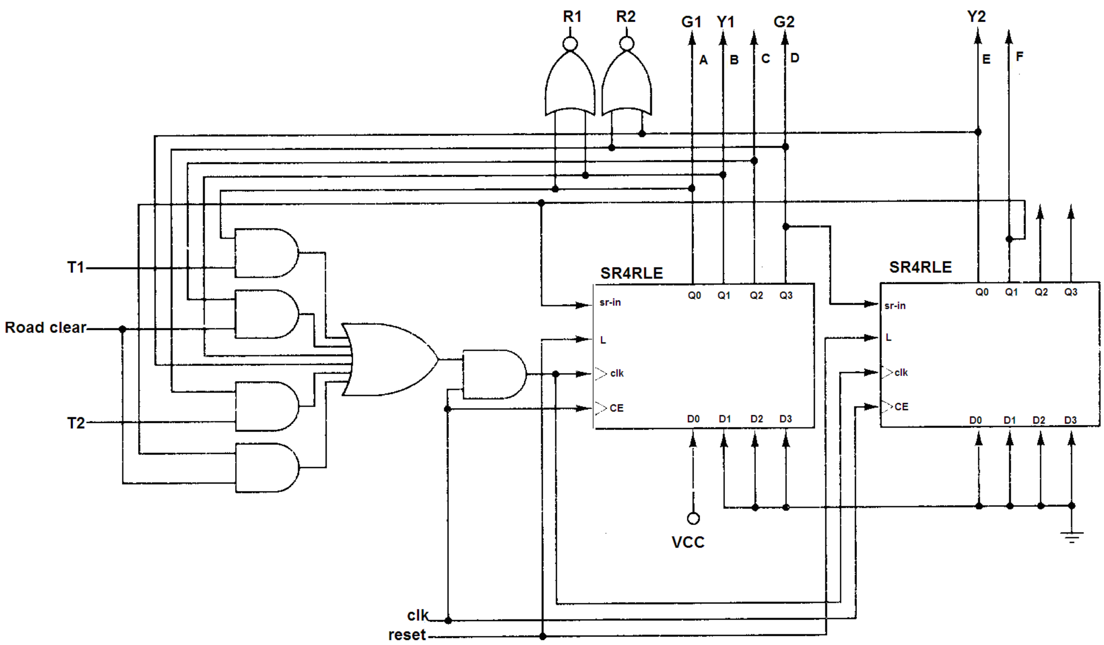


Fig .(13) traffic signal control unit logic diagram

3. Simulation Result

Figure (15) shows the overall schematic design for the controller of one-lane road traffic light as we obtained it by using Xilinx ISE Design suite 13.2.

to obtain the test bench analysis program for our design we assume the timing unite in **ns** , the sensor1 trigger signal on equal 1 and off equal 0,the sensor2 trigger signal on equal 1 and off equal 0, reset on equal 1 and reset off equal 0, and the clock input signal is a square signal in ns . As shown in the simulation wave form analyses output in **Figure (14)**.

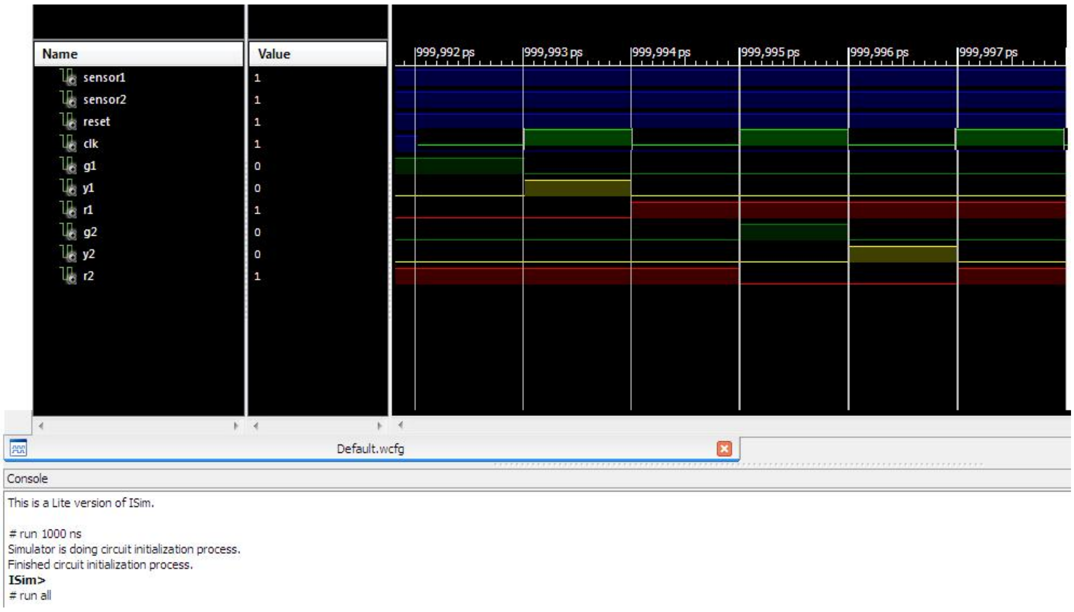


Fig .(14) Simulation result for one-lane traffic light controller

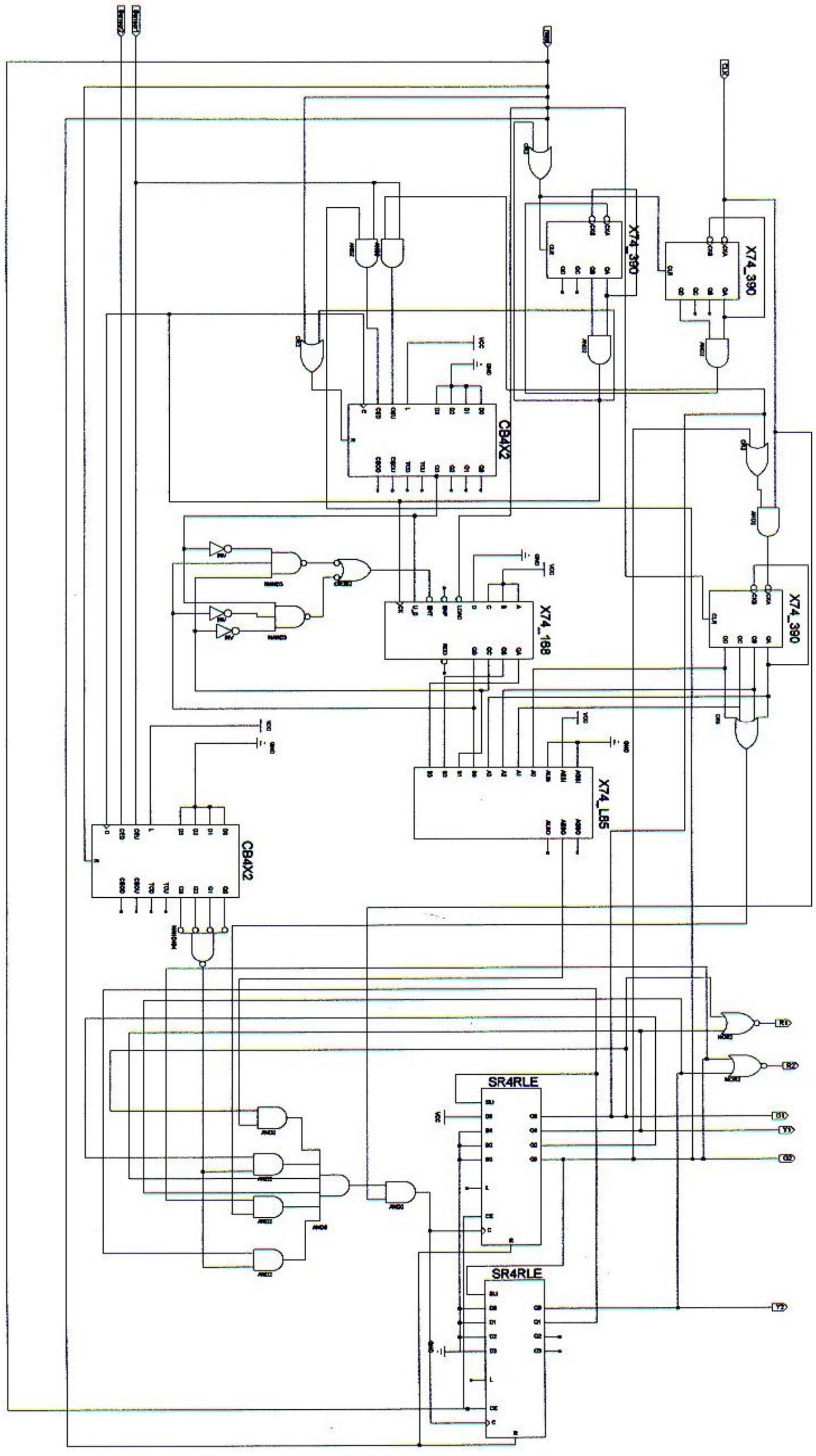


Fig .(15) Schematic Design of the One-Lane Traffic Controller System

4. Conclusion

To improve traffic light control system is essential because the need for the safety and efficiency of transportation. CPLD has been extensively used for custom made circuits. That is why they are perfect for designing traffic light control systems. We achieve by this design that the obtained of an adaptive controller to coordinate traffic signal at the two ends of one-lane road to support two-way traffic is obtained by using **CPLD (XC9500XL).** Analysis the design by using **Xilinx ISE** suite module **13.2**.

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