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Quadratic-Boost-Zeta Converter Based on Coat Circuit for High Voltage Gain Applications

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Abstract

This paper proposes a DC-DC step-up converter with a high voltage gain for solar and fuel cell systems. This converter combines a Zeta converter with one basic cell of the coated circuit and a Quadratic-Boost converter by a high-frequency transformer. The outputs of these two converters are connected in a series to boost the output voltage of the combined DC-DC converter. The proposed converter not only can achieve higher voltage gain but also acquire lower voltage stress on the semiconductor devices. Therefore, the devices with lower conduction resistances. Moreover, the circuit is made so that the outputs of each part of the converter keep the same properties as those of the converter that came before the combination, ensuring that each converter's known benefits are maintained. The proposed topology has one switch, which keeps the number of components low. The simulation of 240-watt, input voltage 30-volt, and 100kHz using the PLECS program is obtained to confirm the theoretical analysis of the proposed converter.

Keywords: High gain; Integrated Converter; Isolated Zeta Converter; Quadratic Boost Converter

1. Introduction

In recent years, there has been a rise in the investigation of new energy sources because of the growing concern over global warming, the environment, and energy consumption [1]-[3]. Alternative ways to generate electricity, like solar and fuel cell systems, are becoming more and more practical [4]-[5]. However, due to the low output voltage of photovoltaics, in most cases, 12V-60V, a significant step-up is needed to increase the voltage for particular applications [6]. For example, in grid-connected applications. Grid-connected power systems run at about 360–400 V [7]. However, in the classical boost converter, an increase in duty cycles to near unity is required to approach a high voltage gain. As a result, there are significant issues, including high voltage stress through the switch and diode, terrible diode reverse recovery, and intense current ripple.

Additionally, the converter efficiency is significantly decreased by the MOSFET equivalent series resistance (ESR), which considerably increases when combined with the ESR of the inductor and capacitor.

Many studies have been done to acquire a high voltage conversion ratio, such as using cascade or stack structures, switched capacitors, and coupled inductors. transformers, voltage multipliers (VMs), and coat circuits. Large transient currents will reduce the service life of the equipment, which is a problem for converters with switched capacitors [8]-[10]. Based on several voltage multipliers, high-voltage gain converters have been presented. With the help of voltage multipliers, the voltage gain of these converters can be made much better, and the voltage stress across switching devices can be greatly reduced [11]-[13]. However, when using multipliers with conventional converters, the high transient currents cause a large conduction loss [13]. The other approach, suggested by Salehi et al. [14] and Bhaskar et al [15], uses stacking or cascading converters. The stack or cascade converter uses more than two converters linked in parallel or series to improve the voltage gain. also requires many power switches, resulting in more loss, low efficiency, and complex control. In[16]-[19], A coupled inductor or transformer needs a high turn ratio to get a high gain, which can cause so much conduction loss. The coupled inductor's

size and weight can also rise. A major problem with these converters is that the leakage inductance causes high voltage stress at the main switch. Snubber is typically used to reduce voltage stress. However, because of the resistor, the R snubber loses some power. High step-up converters based on zeta converters are suggested in [20]. In the circumstances described above, it would be good to combine the advantages methods, i.e., The stacking, cascading layers, and voltage multipliers, together while maintaining high voltage gain without reducing the converter's efficiency [21]. This work proposes that a high step-up converter can be made by cascading and stacking configurations of two well-known Quadratic -boost converters and a Zeta converter with one basic cell of a coated circuit. This converter gets the benefits of both a Zeta converter with one basic cell of the coat circuit and a Quadratic-boost converter, which is low output and input current ripple. Additionally, it uses one switch only and the voltage of the diodes and switch is lower than the output voltage of the proposed converter. Therefore, it is possible to utilize diodes and switches with low on-resistance. It can reduce the converter's overall cost while significantly increasing its efficiency.

2. The Operation Principle of the Proposed Converter

Fig.1 shows the proposed converter. It uses only one switch to combine the Zeta converter with the one basic cell of the coat circuit, and a quadratic boost. The quadratic-boost converter has three diodes (D_1- D_3), one inductor called L_1, one transformer magnetizing inductance L_M, one switch called SW, and an input source V_{in} and two capacitors C_1 and C_5.

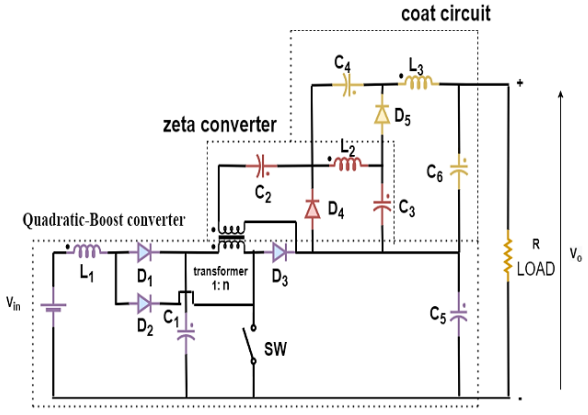


Figure 1. The proposed converter circuit

The Zeta converter with one basic cell of the coat circuit is made up of four capacitors (C_2, C_3, C_4, and C_6), two diodes (D_4 and D_4), and two inductors (L_2 and L_3). The proposed converter's output and input ports are connected to inductors (L_1 and L_3). The proposed converter's output and input ports are connected to inductors (L_1 and L_3). This may help to explain why the proposed converter has a low ripple current in both the output and input ports.

The following presumptions are taken into account to simplify the analysis of the presented converter:

1. All the components are considered ideal.
2. The input and output current is continuous due to using a large inductor in the input and outsides.
3. The capacitances of all capacitors are big enough, so the voltage ripple across them can be neglected.

In continuous conduction mode (CCM), there are three operating modes as follows:

(Mode1 Fig. 2(a) [t_0<t<t_1]): During this period, the diode D_2 and the switch SW are ON state, and the Diodes D_1, D_3, D_4, and D_5 are OFF state. The voltage source and the capacitor C_1 constitute four loops: first, through the main switch SW.the voltage source charges the inductor L_1. Second, the capacitor C_1 charges the inductor L_M. Third, the capacitor C_3 and the inductor L_2 are charged by the capacitor C_1 and the capacitor C_2. Finally, capacitors C_1, C_2, and C_4 charge the inductor L_3 and the capacitor C_6. The capacitors $C_1, C_2, C_4,$ and C_6 deliver power to the load. The capacitors C_3 and C_6 are charged and the capacitors C_1, C_2, C_4, and C_5 are discharged. The currents i_{L1}, i_{Lm}, i_{L2}, and i_{L3} increase linearly.

By using KVL, inductor voltages are as follows:

$$V_{L1} = V_{in} \quad (1)$$

$$V_{LM} = V_{C1} \quad (2)$$

$$V_{L2} = nV_{C1} + V_{C2} - V_{C3} \quad (3)$$

$$V_{L3} = nV_{C1} + V_{C2} + V_{C4} - V_{C6} \quad (4)$$

Where *n* is the turn ratio of the transformer Ns/*Np*

(Mode2 Fig. 2(b);[t_1<t<t_2]): During this period, the switch SW, the diodes D_2, D_3, and D_4 are turned OFF at t_1, and then the diodes D_1 and D_5 begin to turn ON. The process continues discharging the inductance L_1, L_M, L_2 and L_3. Fig. 2(b) illustrates four loops: first, the V_{in} and the inductor L_1 charge the capacitor C_1. Second, the inductors L_M charges the capacitors C_2 and C_4 through the capacitor C_3 and the diode D_5. Three, the capacitor C_4 is charged by the inductor L_2 across the diode D_5. Finally, the capacitor C_3 and inductor L_3 charge the capacitor C_6 and the delivered power to the load with a capacitor C_5. The capacitors C_1, C_2, C_4, and C_6 are charged and the capacitors C_3 and C_5 are discharged. Consequently, the currents i_{L1}, i_{Lm}, i_{L2}, and i_{L3} decrease linearly.

$$V_{L1} = V_{in} - V_{C1} \quad (5)$$

$$V_{L2} = nV_{c1} + V_{C2} - V_{C3} = -V_{C4} \quad (6)$$

$$V_{L3} = V_{c3} - V_{c6} \quad (7)$$

(Mode3 Fig. 2(c)[t_2<t<T_s]): During this period, the diode D_2 and the switch SW are in an OFF state. The diodes D_1, D_3, D_4, and D_5 are ON state. The discharging of the inductors L_1, L_M, L_2, and L_3 keeps on, and Fig. 2(C) illustrates six loops: First, the V_{in} and the inductor L_1 are continuous charging capacitor C_1. Second, the capacitor C_5 is charged by the V_{in}, the inductor L_1 and the inductor L_M. Third, through the diode D_4, the capacitor C_2 is charged by the inductor L_M Fourth, the capacitor C_4 is charged by the inductor L_M through the diode D_5 and the capacitor C_3. Five, through diode D_5, the inductor L_2 charges the capacitor C_4. Finally, the capacitor C_6 with inductor L_3 and the capacitor C_3 deliver power to the load. The capacitors C_1, C_2, C_4, and C_5 are charged and the capacitor s C3 and C_6 are discharged. Hence, the currents i_{L1}, i_{LM}, i_{L2}, and i_{L3} decrease linearly.

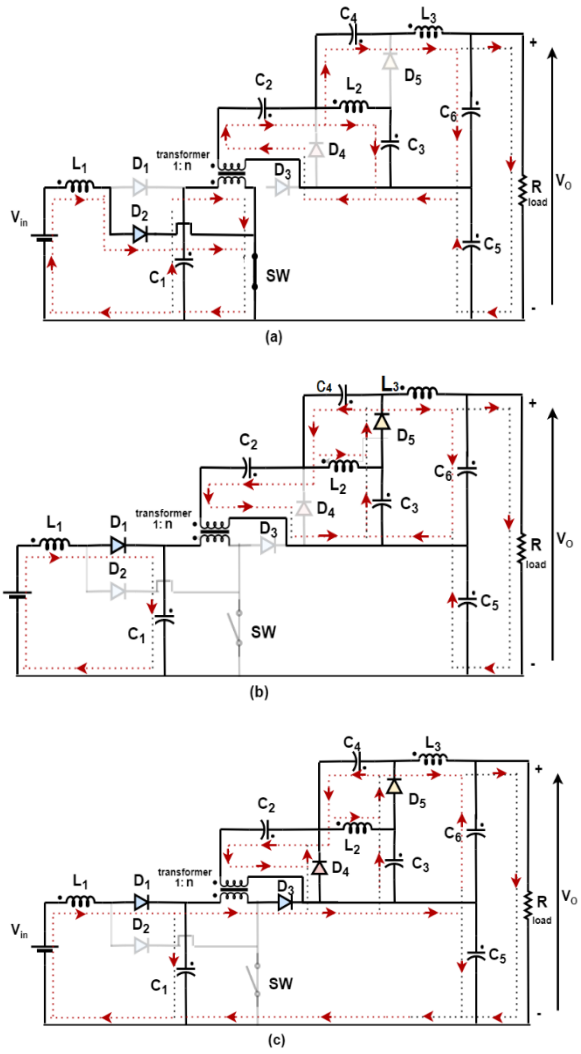


Figure 2. Modes of operation of the proposed converter (a)Mode 1, (b) Mode 2, (c) Mode 3

$$V_{L1} = V_{in} - V_{c1} \quad (8)$$

$$V_{LM} = V_{c1} - V_{c5} \quad (9)$$

$$V_{L2} = -V_{c3} = -V_{c4} \quad (10)$$

$$V_{L3} = V_{c3} - V_{c6} \quad (11)$$

$$V_{sec} = -V_{c2} = n(V_{c1} - V_{c5}) \quad (12)$$

3. Study State Analysis

A-Voltage Gain

By using the IVSB principle on the inductors L_1, L_M, L_2, and L_3, and using Equations (1-12). The following equations can be obtained:

$$\int_0^{DTs} V_{L1}\,dt + \int_{DTs}^{Ts} V_{L1}dt = 0$$
$$V_{in} * D + (V_{in} - V_{C1}) * (1 - D) = 0 \quad (13)$$

$$\frac{V_{C1}}{V_{in}} = \frac{1}{(1-D)} \quad (14)$$

Where D is the duty cycle.

$$\int_0^{DTs} V_{LM}\,dt + \int_{DTs}^{Ts} V_{LM}dt = 0$$
$$V_{C1} * D + (V_{C1} - V_{C5}) * (1 - D) = 0 \quad (15)$$

$$\frac{V_{C5}}{V_{C1}} = \frac{1}{(1-D)} \quad (16)$$

$$\int_0^{DTs} V_{L2}dt + \int_{DTs}^{Ts} V_{L2}dt = 0$$
$$(nV_{c1} + V_{C2} - V_{C3}) * D + (-V_{C3}) * (1 - D) = 0$$
$$(nV_{c1} * D + V_{C2} * D - V_{C3} = 0$$
$$(nV_{c1} * D - n(V_{c1} - V_{c5}) * D - V_{C3}) = 0 \quad (17)$$

$$\frac{V_{C4}}{V_{C1}} = \frac{V_{C3}}{V_{C1}}\ \frac{nD}{(1-D)} \quad (18)$$

$$\int_0^{DT} V_{L3}\,dt + \int_{DT}^{T} V_{L3}dt = 0$$
$$(nV_{C1} + V_{C2} + V_{C4} - V_{C6}) * D + (V_{c3} - V_{c6}) * (1 - D) = 0$$
$$(nV_{c1} * D + V_{C2} * D + V_{C3} - V_{C6}) = 0$$
$$(nV_{c1} * D + -n(V_{c1} - V_{c5}) * D + V_{C3} - V_{C6}) = 0 \quad (19)$$

$$\frac{V_{C6}}{V_{C1}} = \frac{2nD}{(1-D)} \quad (20)$$

$$V_o = V_{c5} + V_{c6} \quad (21)$$

The voltage gain of the proposed converter is

$$M = \frac{V_0}{V_{in}} = \frac{1+2nD}{(1-D)^2} \quad (22)$$

The proposed converter's gain in voltage would be 12 times greater than the input voltage at duty cycle 50% and a transformer ratio = 2. Fig. 3 shows some important waves of (CCM).

B-Voltage and Current Stress of Components

The voltage of switch SW, and the diodes ($D_1 - D_5$) can be represented by the symbols V_{SW}, V_{D1}, V_{D2}, V_{D3}, $V_{D4,}$and V_{D5}; respectively. According to Fig. 1 and 3, the following equations can be obtained:

$$\left.\begin{aligned} V_{SW} &= V_{c5} \\ V_{SW} &= \frac{1}{(1-D)^2} V_{in} \end{aligned}\right\} \quad (23)$$

$$\left.\begin{aligned} V_{D1} &= V_{c1} \\ V_{D1} &= \frac{1}{(1-D)} V_{in} \end{aligned}\right\} \quad (24)$$

$$\left.\begin{aligned} V_{D2} &= V_{c5} - V_{c1} \\ V_{D2} &= \frac{1}{(1-D)} V_{in} \end{aligned}\right\} \quad (25)$$

$$\left.\begin{aligned} V_{D3} &= V_{c5} \\ V_{D3} &= \frac{1}{(1-D)^2} V_{in} \end{aligned}\right\} \quad (26)$$

$$\left.\begin{aligned} V_{D4} &= nV_{c1} + V_{c2} \\ V_{D4} &= nV_{c1} - n(V_{c1} - V_{c5}) \\ V_{D4} &= nV_{c5} \\ V_{D4} &= \frac{n}{(1-D)^2} V_{in} \end{aligned}\right\} \quad (27)$$

$$\left.\begin{aligned} V_{D5} &= -V_{c3} + nV_{c1} + V_{c2} + V_{c4} \\ V_{D5} &= nV_{c1} - n(V_{c1} - V_{c5}) \\ V_{D5} &= nV_{c5} \\ V_{D5} &= \frac{n}{(1-D)^2} V_{in} \end{aligned}\right\} \quad (28)$$

Assuming that the converter efficiency of the converter is 100%.

$$\left.\begin{aligned} P_{in} &= P_{out} \\ V_{in} * I_{L1} &= V_O * I_0 \end{aligned}\right\} \quad (29)$$

$$I_{L1} = \frac{1+2nD}{(1-D)^2} I_o$$

The average current of the proposed converter can be obtained as:

$$I_{Tp} = (1-D) I_{L1} \quad (30)$$

$$I_{D2} = D \frac{1+2nD}{(1-D)^2} I_o \quad (31)$$

$$I_{D1} = \frac{1+2nD}{(1-D)} I_o \quad (32)$$

$$I_{D3} = I_{D4} = I_{D5} = I_{L2} = I_{L3} = I_O \quad (33)$$

$$I_{SW} = I_{D2} + I_{Tp} - I_O \quad (34)$$

4. Parameters Design

A-Inductance Design

The current ripple is almost always planned ahead of time in practical uses, The inductors L_1, L_M, L_2, and L_3 can be obtained as:

$$\left.\begin{aligned} V_{in} &= L_1 \frac{\Delta I_{L1}}{DT} \text{ from on state} \\ L_1 &\geq \frac{V_{in} * D}{\Delta I_{L1} * f} \end{aligned}\right\} \quad (35)$$

$$\left.\begin{aligned} V_{C1} &= L_M \frac{\Delta I_{TP}}{DT} \text{ from on state} \\ L_M &= \frac{V_{in} * D}{\Delta I_{TP} * f * (1-D)} \end{aligned}\right\} \quad (36)$$

$$\left.\begin{aligned} V_{C3} &= L_2 \frac{\Delta I_{L2}}{(1-D)T} \text{ from off state} \\ L_2 &\geq \frac{n * V_{in} * D}{\Delta I_{L2} * f * (1-D)} \end{aligned}\right\} \quad (37)$$

$$\left.\begin{aligned} V_{C4} - V_{C6} &= L_3 \frac{\Delta I_{L3}}{(1-D)T} \text{ from off state} \\ L_3 &\geq \frac{n * V_{in} * D}{\Delta I_{L3} * f * (1-D)} \end{aligned}\right\} \quad (38)$$

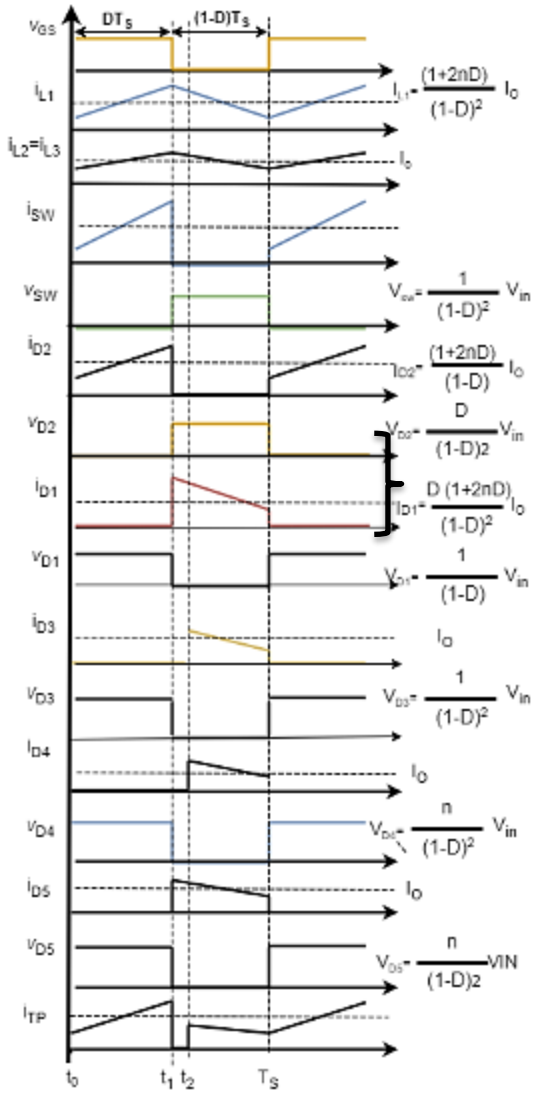


Figure 3. Some important waveforms for the proposed converter

B-Capacitors Design

The voltage ripple is almost always planned ahead of time in practical uses. The capacitors (C_1- C_6) can be obtained as

$$I_{c1-on} = I_{TP} = (1-D)I_{L1} = C_1 \frac{\Delta V_{C1}}{DT}$$

$$C_1 \geq \frac{I_{L1} * D}{\Delta V_{C1} * f} = \frac{D}{\Delta V_{C1} * f} * \frac{1+2nD}{(1-D)} I_o \quad (39)$$

$$I_{c5-on} = I_O = C_5 \frac{\Delta V_{C5}}{DT}$$

$$C_5 \geq \frac{V_O * D}{R * \Delta V_{C5} * f} \quad (40)$$

$$I_{c2-on} = I_{L2} + I_{L3} = 2I_0 = C_2 \frac{\Delta V_{C2}}{DT}$$

$$C_2 \geq \frac{2 * V_O * D}{R * \Delta V_{C2} * f} \quad (41)$$

$$I_{c3-on} = I_{L2} = I_O = C_3 \frac{\Delta V_{C3}}{DT}$$

$$C_4 = C_3 \geq \frac{V_O * D}{R * \Delta V_{C3} * f} \quad (42)$$

$$C_6 * \Delta V_{c6} = 0.5 * \frac{T}{2} * \frac{\Delta I_{L3}}{2}$$

$$C_6 \geq \frac{\Delta I_{L3}}{8 * f * \Delta Vc6} \quad (43)$$

5. Comparison

Table 1 shows the main parameters that can be used to compare the proposed converter to other topologies. Even though the displayed topology consists of a single switch and a simple method for controlling it, it still needs a lot of diodes. But it stands out from other converters because it has the highest voltage ratio and, except for the structure in [18], the lowest voltage across the switches and diodes. The topology in [18], the input and the output current ripple is high. Moreover, it needs two active switches. Also, in [19] and [21], the output diode voltage and the switch voltage are higher than in the proposed converter. The presence of the boost converter's input inductor is responsible for the reduced input current ripple on the input side. Also, the proposed converter has an output inductor which is one of the components that help to reduce the current ripple on the output side.

Table 1 Comparison between Proposed Converter and Other Converters

Topologies	**[18]**	**[21]**	**[19]**	**Proposed Converter**
Number of Diodes	3	5	6	5
Number of Switches	2	1	1	1
Gain	$\frac{2+(n\,(2-D))}{1-D}$	$\frac{1+nD}{(1-D)^2}$	$\frac{1+nD}{(1-D)^2}$	$\frac{1+2nD}{(1-D)^2}$
Switch voltage	$\frac{V_o}{2+(n(2-D))}$	$V_O/(1+nD)$	$V_O/(n)$	$V_O/(1+n)$
output Diode Voltage	$\frac{1+n}{2+n*(2-D)}V_o$	$\frac{n}{1+nD}V_o$	$\frac{1+n}{1+nD}V_o$	$\frac{n}{1+n}V_o$
Input Current Ripple	high	low	low	low
Output Current Ripple	high	low	low	low

6. Simulation Results

PLECS has been used to simulate the closed-loop control of the proposed converter, as shown in Fig. 4. The values of the components used in the proposed converter are listed in Table 2 which considers the voltage ripple and the current ripple as $\Delta V_{c1} = 1\%$ of V_{C1}, $\Delta V_{c2.3.4.5} = 0.84\,\%$ of $V_{C2.3.4.5}$ and $\Delta V_{c6} = 0.1\%$ of V_{C6} and the $\Delta I_{L1.2.3} = 30\%$ of $I_{L1.2.3}$.

The voltage stress through the switch SW, the input source, the output voltage, and gate voltage waveforms are displayed in Fig. 5 and 6 as V_{gate}, V_{in}, V_{SW}, and v_O. The output voltage is approximately 360V, and the switch voltage is 120 V at a duty cycle of roughly 50%, consistent with Equations (22) and (23).

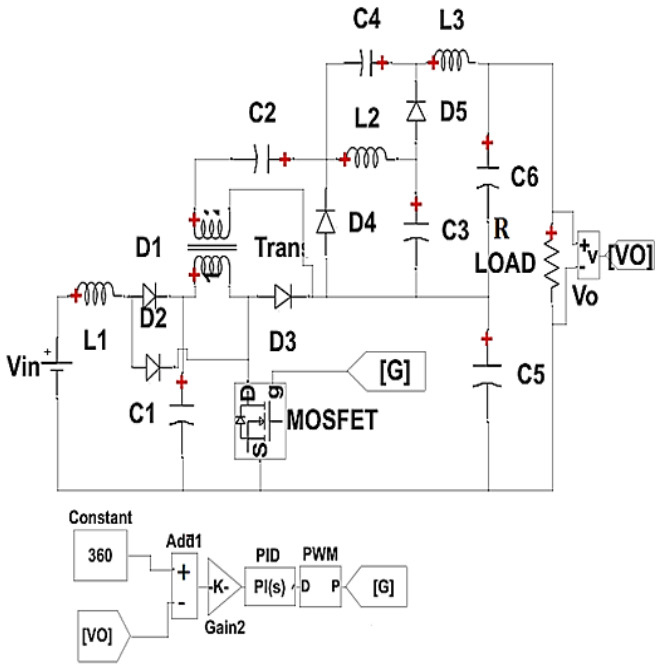


Figure 4. Converter simulation circuit with voltage closed-loop control

Table. 2 Parameters of the Proposed Converter

Number	Name	Value
1	L_1	$63*10^{-6}$ H
2	L_2	$3*10^{-3}$ H
3	L_3	$3*10^{-3}$ H
4	C_1	$33.33*10^{-6}$ F/ 120V
5	C_5	$3.3*10^{-6}$ F/240V
6	C_2	$6.6*10^{-6}$ F/240V
7	C_3	$3.3*10^{-6}$ F/240V
8	C_4	$3.3*10^{-6}$ F/240V
9	C_6	$1*10^{-6}$ F/480V
10	Transformer Magnetizing Inductance (L_m)	$87*10^{-6}$ H
11	R Load	540 ohm
12	Switching frequency (f)	100kHz
13	Input Voltage(v)	30V
14	Turn Ratio(n)	2

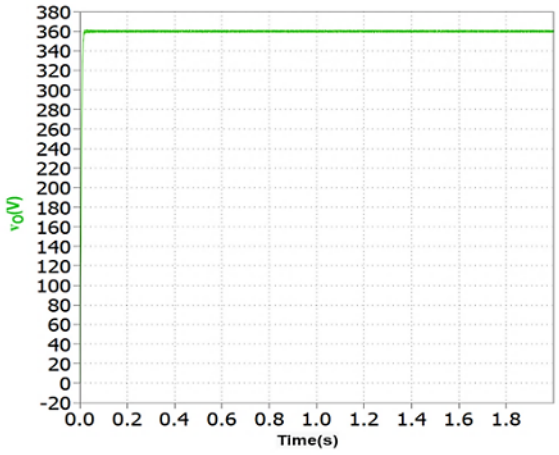


Figure 5. Output voltage

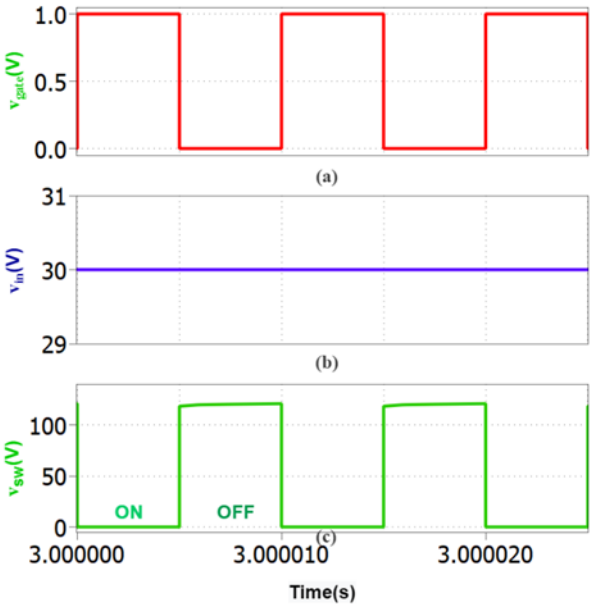


Figure 6. Waveforms of the proposed converter, (a)PWM switch control, (b)Input voltage, (c)Voltage across the switch.

The current waveforms for the inductors L_1. L_2, L_3, transformer primaryi_{TP}, transformer secondary i_{TS}, and switch i_{SW} are shown in Fig. 7 and 8. Approximately 8 A on the average current through inductor L_1, the average currents of inductors L_2 and L_3 are roughly 0.66 A, the average current through the primary transformer was approximately 4 A, and the average current through the switch was approximately 7.34 A, which is consistent with Equations (29), (30), (33), and (34).

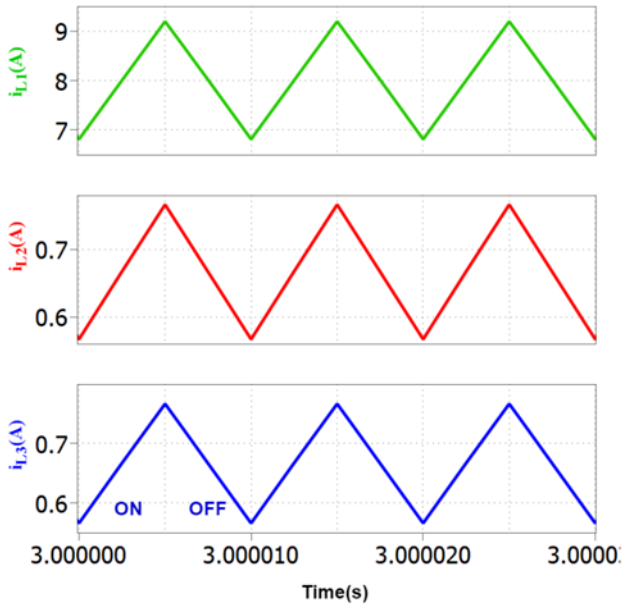


Figure 7. Current waveforms i_{L1}. i_{L2} and i_{L3}

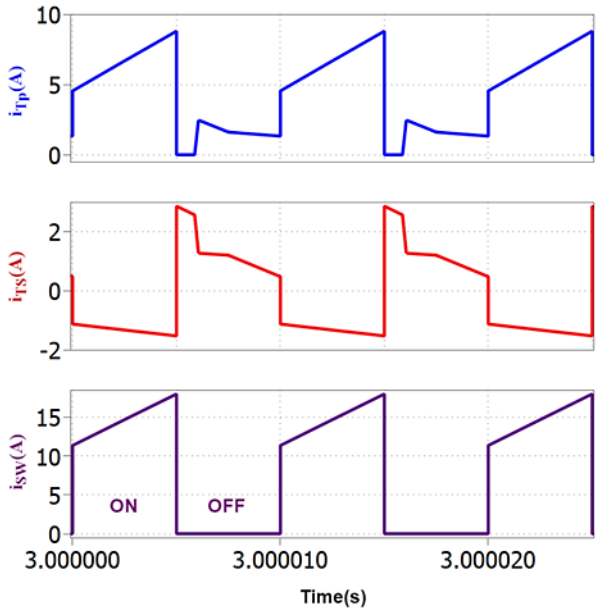


Figure 8. Current waveforms i_{TP}. i_{TS} and i_{SW}

The voltage waveforms of D_1, D_2, D_3, D_4 and D_5 are shown in Fig. 9. V_{D1} and V_{D2} are around 60 V, V_{D3} is approximately 120 V, and V_{D4} and V_{D5} are approximately 240 V. The outcomes of the voltage stress given above are the same as those obtained in Equations (24), (25), (26), (27), and (28).

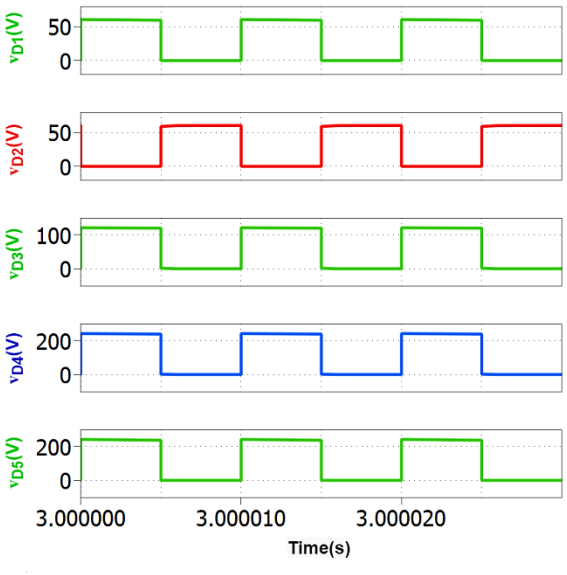


Figure 9. Voltage waveforms v_{D1}. v_{D2} v_{D3} . v_{D4} and v_{D5}

The waveforms of the voltages across the capacitors (C_1- C_6) are shown in Fig. 10. V_{C1} is roughly 60 V, V_{C2}, V_{C5}, V_{C3}, and V_{C4} are all roughly 120, but V_{C6} is roughly 240 V. which is consistent with Equations (14), (16), (18), and (20). The current waveforms of D_1, D_2, D_3, D_4, and D_5 are shown in Fig.11. The average current of the diodes D_1 and D_2 are equal to 4A, and the average currents of the diodes D_3, D_4, and D_5 are roughly 0.66 A.

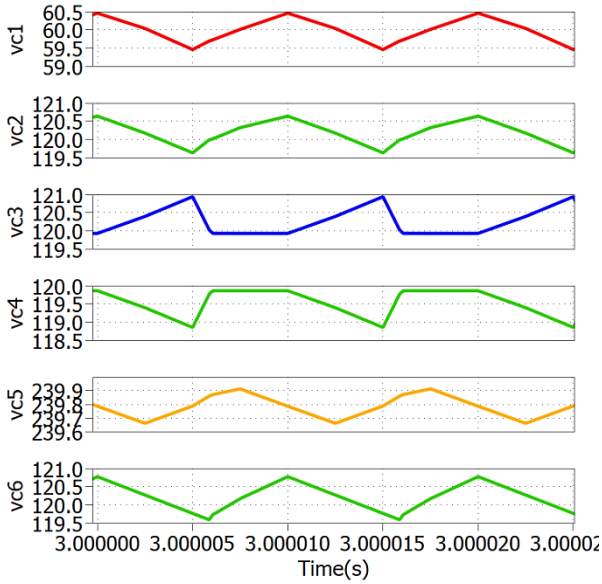


Figure 10. Voltage waveforms v_{C1} . v_{C2} . v_{C3} . v_{C4} . v_{C5} and v_{C6}

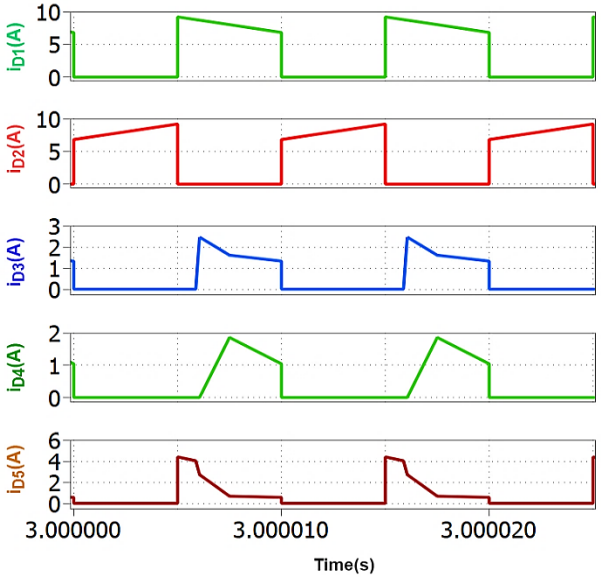
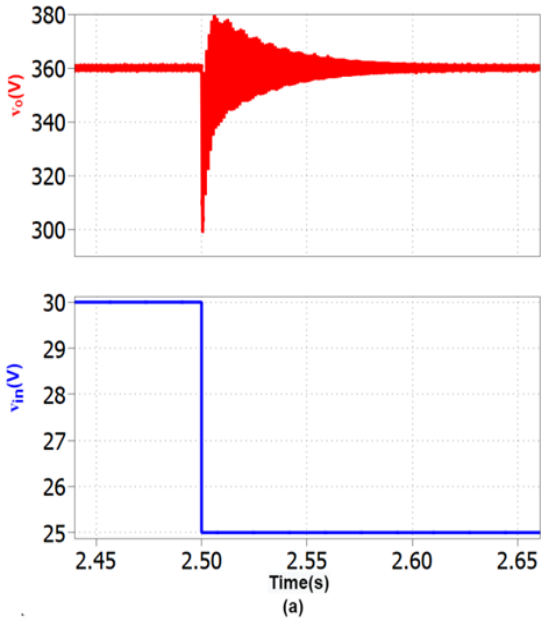


Figure 11. Current waveforms i_{D1}. i_{D2} i_{D3}. i_{D4} and i_{D5}

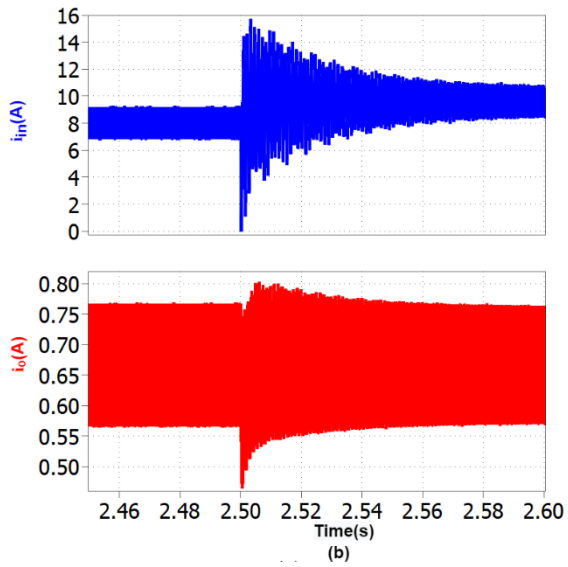
The outcomes of the current given above are the same as those obtained in Equations (31), (32), and (33).

Also, Fig. 12 shows the waveforms for the dynamic performance. Fig. 12(a), 12(b), 12(c), and 12(d) shows i_{in}, i_o, $V_{in,}$ and v_o waveforms as the value of V_{in} is decreasing suddenly from 30V to 25V at time 2.5s and also, increasing suddenly from 30V to 35V at time 2.5s. As shown in Fig. 12(a) and 12(b), as the input voltage decreases, the output voltage decreases slightly, with a down shoot about 60V. It gets to the rated value in about 0.16s. Figures 12(c) and 12(d) show that as input voltage increases, the output voltage increases slightly, with an overshoot of about 68 V. It can also reach a steady state in about 0.1s.

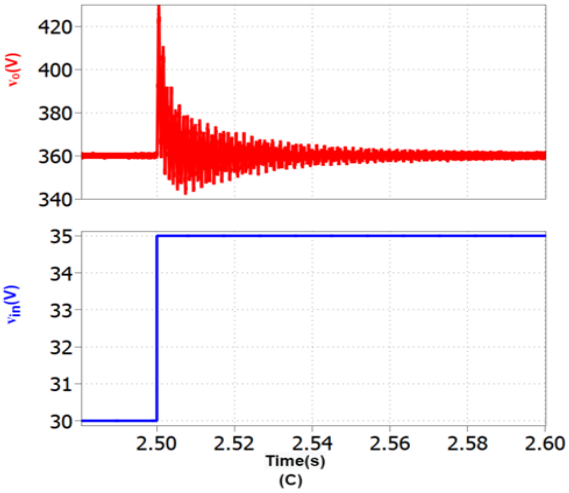
Fig. 13(a), 13(b), 13(c), and 13(d) show i_{in}, i_o, and V_{in} waveforms as the load resistance changes from 700Ω to 540Ω at time 2.5s and, also changes from 540Ω to 700Ω at time 2.5s. As shown in Fig.13(a) and 13(b), the value of v_o is decreasing slightly, with a down shoot about 22 V. It gets to the rated value in about 0.08s. In Fig. 13(c) and 13(d), the value of v_o is increasing slightly, with an overshoot of about 22 V. It can also reach a steady state. According to the closed-loop control scheme, the dynamic testing waveforms have demonstrated that the dynamic response is quick and that there is a minor voltage overshoot and downshoot.



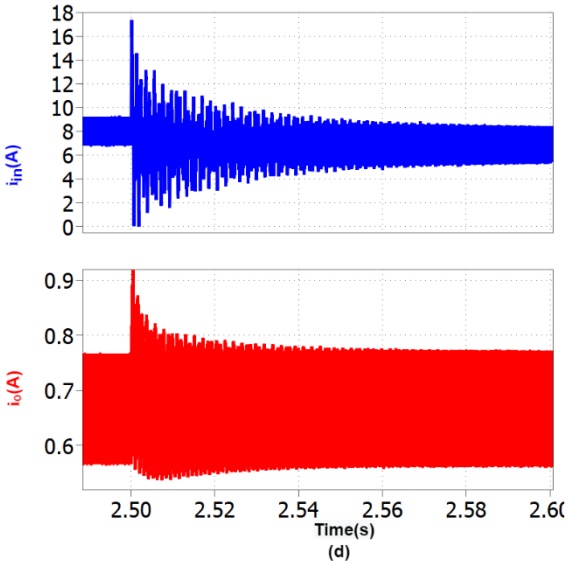
(a) Output and input voltage wavefrom when the value of Vin changes from 30V to 25 V



(b) Output current and input wavefrom when the value of Vin changes from 30V to 25 V

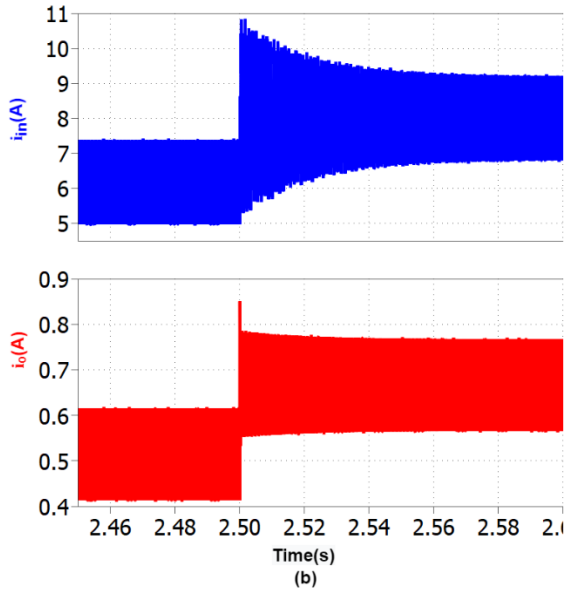


(c) Output and input voltage wavefrom when the value of Vin changes from 30V to 35 V

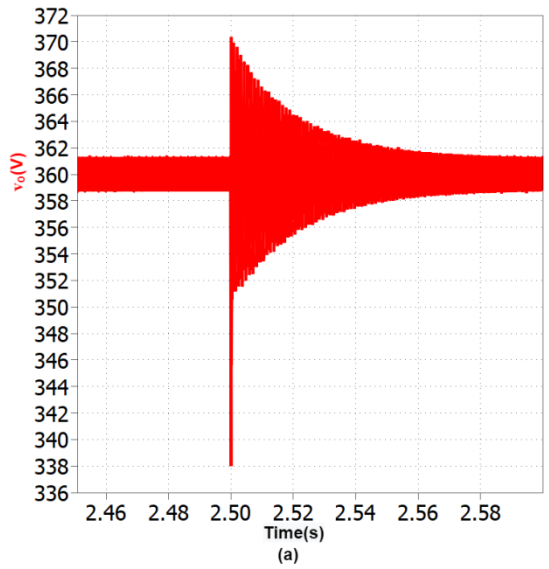


(d) Output current and input wavefrom when the value of Vin changes from 30V to 35 V

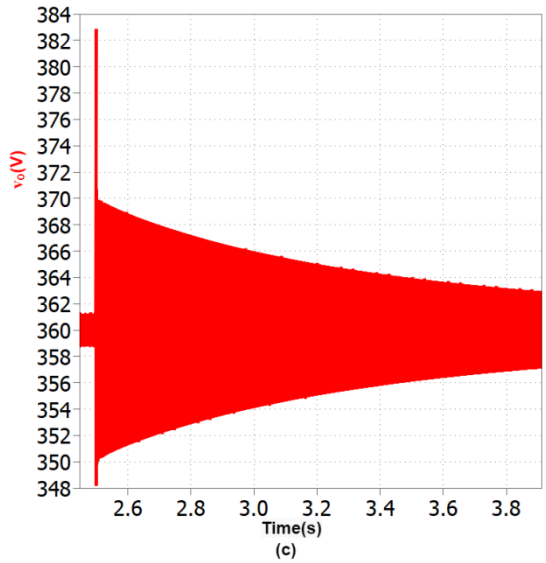
Figure 12. Converter dynamic response



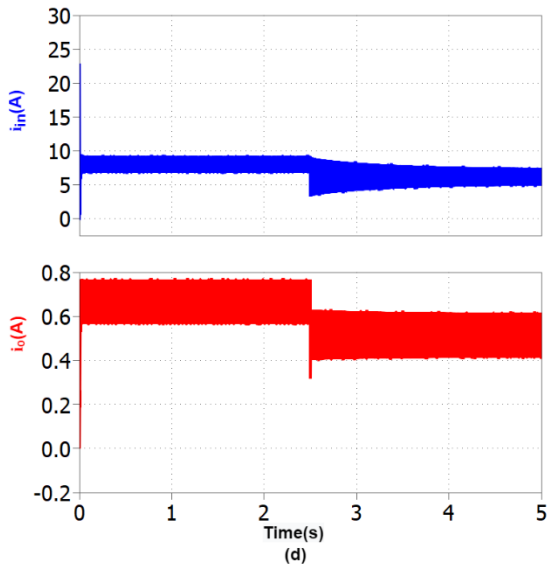
(b) Output and input current waveforms when the value of the R is changing from 700 Ω to 540 Ω



(a) Output voltage wavefrom when the value of the R is changing from 700 Ω to 540 Ω



(c) Output wavefrom when the value of the R is changing from 540 Ω to 700 Ω



(d) Output and input current waveforms when the value of the R is changing from 540 Ω to 700 Ω

Figure 13. Converter dynamic response

7. Conclusions

In this paper, the Zeta converter with one basic cell of the coat circuit and quadratic-boost converter are successfully combined by a high-frequency transformer with a turns ratio equal to 2. It is driven by a single switch, which can simplify the circuit structure and achieve a high voltage gain. The output voltage value is 360V which is greater than the input voltage about 12 times when the duty cycle is equal to 50%. The circuit is analyzed and designed with a frequency of 100 kHz, output voltage of 360 volts, input voltage of 30 volts, and output power of 240 watts. Also, the converter is tested using the PLECS program, and the prototype's dynamic performance has been analyzed using a closed-loop system with different load resistors. In conclusion, a high voltage gain has been achieved. Also, the voltage across the diodes and power switch is low, and the output and input current ripple about 1.2% and 30% respectively; also, it is possible to use the power switch with low on-resistance, which reduces losses and increases efficiency.

Conflicts of interest

The authors declare that there are no conflicts of interest regarding the publication of this manuscript

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Author Contribution Statement

All authors contributed to formulating the research topic and simulation model to resolve the issue and achieve the study objective.

Turki K. Hassan supervised the final results of the manuscript.

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