Bandwidth Extension in Cascaded Single-Stage Distributed Microwave Amplifier

Prof. Dr. Ali A. Ali Electrical Engineering Department University of Technology, Baghdad, Iraq Asst. Lect. Azad R. Kareem Control & Computer Engineering Department University of Technology, Baghdad, Iraq

Abstract

In this paper the principles of wideband microwave amplifier will be highlighted. Special attention goes to the design methodology of high-gain cascaded single-stage distributed amplifiers (CSSDA). Alternation to the basic design including the use of "cascode" gain cells is then discussed. This is a new technique for enhancing the bandwidth of the amplifier. The final design is implemented using microwave office program. A four-stage CSSDA with and without cascode cells were tested in order to demonstrate the validity of the proposed method.

الخلاصية

يسلط هذا البحث الضوء على مبادء المضخمات المايكروية ذات النطاق الترددي الواسع الذي يستخدم في دوائر الاستقبال للعديد من الانظمة الراديوية او المايكروية كانظمة الاتصالات البصرية و الاتصالات عبر الاقمار الصناعية. يذهب اهتمام خاص الى طريقة تصميم المضخمات عالية الكسب التي تعتمد على مبدأ الربط التراكمي لمضخمات احادية المرحلة (CSSDA) التي هي احد اهم الطرائق المعتمدة في هذا المجال. اقترح تصميم جديد في البحث و ذلك بأضافة خلايا من نوع " cascode" الى دائرة المضخم ، هذه الخلايا تساعد على تقليل قيمة المتسعات الطفيلية للترانسستورات التي تظهر في الترددات العالية والتي لها تاثير كبير على تضييق الحزمة الترددية التى يستجيب لها النظام . سميت وكانت النتائج تشير الى ان الطريقة الجديرة تعطي استخدام برنامج " accober الخلايا تساعد على تقليل قيمة المتسعات الطريقة المقترحة " CSCSDA" وقد اختبرت باستخدام برنامج " microwave office" الخاص بالانظمة المايكروية وكانت النتائج تشير الى ان الطريقة الجديدة تعطي استجابة ترددية قريبة جدا من الحسابات النظرية في حين ان الطرائق الطريقة تستجيب دائما لحزمة الله بين المتسعات الطولية المايكروية المايكروية

1. Introduction

Microwave amplifier design is an important part of many microwave electronic systems. The amplifier can be divided according to their functions into ^[1]: small-signal amplifier, large-signal amplifier, low-noise amplifier, high-gain amplifier, and high power amplifier. They are also classified according to their bandwidth into: narrowband and wideband (broadband) amplifiers. The ideal broadband microwave amplifier would have constant gain and good impedance matching of mainly capacitive input impedance. There are several techniques to design the broadband amplifiers; each has its drawbacks and advantages, which can be summarized by:

- **1. Compensated Matching Technique:** input and output matching circuits can be designed to compensate the gain roll off, but generally at the expense of the input and output match.
- **2. Resistive Matching Technique:** good input and output matching can be obtained with a corresponding loss in gain and increase in noise figure.
- **3. Negative Feedback Technique:** resistive feedback can also be used for designing a broadband amplifier. The effect of a feedback resistor between the gate and drain of a FET (or between the base and collector of a BJT) is to lower the input and output impedance, broaden the gain curve, and improve the stability. The drawback is resistive coupling between the bias circuits, as well as overall lower gain than for reactively matched amplifiers.
- **4. Balanced Amplifier Technique:** two amplifiers having 90° couplers at their input and output can provide a very good matching. The gain is equal to that of a single amplifier. An additional disadvantage is the size of the circuit and the fact that a large part of the system is taken by passive circuits. This is very costly in monolithic integrated circuit implementations.
- **5. Distributed Amplifier (DA) Technique:** several transistors are cascaded together along a transmission line, giving good gain, matching, and noise figure over a very wide bandwidth. Thus distributed amplifiers are used in many radio-frequency and high-data rate communication systems including satellite transceivers, pulsed radar system, optical receivers, etc ^[2].

The objective of this paper is to develop a design methodology of a high-gain broadband amplifier which is one of the challenging aspects in emerging high-data rate microwave communication system.

2. Theory of Distributed Amplification

The concept of distributed amplification was first proposed in 1948^[3] as a means of improving the gain-bandwidth product of wide-band amplifiers by adding the transconductance of individual tubes while separating their capacitances. Thus, it is possible

to achieve an amplifier with bandwidth greater than the one that resulted by a simple parallel connection of the tubes. Since then many researchers implemented distributed amplifiers (DA's) using different transistor technologies ^[4,5,6,7,and8]. Basic structure of N-stage distributed amplifier is shown in **Fig.(1)**. It consists of a pair of input and output transmission lines coupled by transconductance of the active devices. The transmission lines are formed using lumped inductors and are referred to as the gate and drain lines. The gate line is periodically loaded by the transistor gate-source capacitance (Cgs) and is terminated by its characteristic impedance (Zo) at the end. On the other hand, the drain line is loaded by the drain-source capacitances (Cds).



Figure (1) N-Stage Distributed Amplifier

The bandwidth of the amplifier is limited by the cutoff frequencies of the LPF segments of the transmission lines ^[9].

$$w_{c} = \frac{2}{\sqrt{LC}} \qquad (1)$$

where L = Lg (or Ld) and C = Cgs (or Cds). The power gain of the amplifier is given by:

where $g_m = transconductance per transistor$.

The limited gain-bandwidth is the only drawback of this amplifier ^[2]. High gain can be achieved by another topology based on cascading several single stage distributed amplifiers (CSSDA), see **Fig.(2**). It is essentially a cascade connection of single-stage distributed amplifiers with the omission of idle gate and drain termination for the intermediate stages ^[10]. The inductors Lg's and the gate capacitance Cgs of T1 form the input artificial transmission

line where as the inductors Ld's along with the drain capacitance Cds of TN serves as the output artificial line. These input and output lines match the amplifier to the source and load impedance Zo.



Figure (2) N-Stage CSSDA

The available power gain expression for the CSSDA is given by ^[10]:

The gain advantage over the classical distributed amplifier may be achieved with appropriate range of parameter values for the inter-stage impedance Z_I i.e.

$$\mathbf{Z}_{\mathbf{I}} \geq \sqrt[(N-1)]{\mathbf{N}} / \mathbf{g}_{\mathbf{m}}$$
 (4)

3. The proposed Cascaded Single Cascode Stage Distributed Amplifier (CSCSDA)

All the equations given in section two were determined using unilateral (Cdg=0) version of the FET equivalent circuit, which is practically unobtainable case. With the existence of Cdg and according to Miller's theorem ^[11], the value of Cgs and Cds will be shifted to:

$$Cg'_{s} = Cg_{s} + Cd_{g}(1 - A)$$

$$Cd'_{s} = Cd_{s} + Cd_{g}(1 - \frac{1}{A})$$
(5)

where $A = g_m Z_0$ is the gain factor.

By adding a common-gate amplifier section to the drain line of a common-source amplifier stage, a very useful amplifier circuit results. It is known as the cascode configuration. The name cascode is short for "cascaded cathode" and dates back to the days of the vacuum tubes since the anode of the first tube feeds the cathode of the second.

A cascode stage was added to the conventional DA ^[12] to decrease the variation in the capacitance seen by the transmission lines, which is caused by Miller's effect. Also the cascode stage improves the gain and provides isolation to the signal in the drain line coupling back to the gate line. **Figure (3 a,b)** show simple gain stages with the parasitic capacitances of the transistor. The effective capacitance in the gate line is larger than Cgs and the effective Zo is less than desired. **Figure (3 c,d)** show the cascode gain stage with the parasitic capacitances. A cascode gain stage helps in reducing the effective capacitance in the gate and drain lines compared with the simple gain stage. This slight variation in capacitance, on both, the drain and gate lines, causes only a slight variation in Zo. As a result, the cascode amplifier can be designed to obtain a wider bandwidth but equal dc gain as compared with the simple common-source amplifier stage. This advantage is taken into consideration to design an alternative topology for the CSSDA based on the cascode amplifier configuration. The new version of distributed amplifier will be defined as "cascaded single cascoded stage distributed amplifier" or "CSCSDA".



Figure (3) a- One Gain Stage of DA, b- Gain Stage with Miller Effect c- Cascode Gain Stage, d- Cascode Gain Stage with Miller Effect

4. Illustrative Design Example

This section illustrates how the cascode gain cells can improve the performance of the CSSDA. **Figure (4)** shows the schematic representation of a 4-stage CSCSDA. The cascode cells affect the bandwidth of the amplifier which is limited by lumped elements of the artificial transmission line (L and the parasitic capacitances of the transistors). The input and output circuits (Lg+Cgs₁ and Ld+Cds_N) possess much larger bandwidth compared with that of the inter-stage loads, therefore their effect may be neglected. Equation (3) is still valid for power gain computation. The CSSDA and CSCSDA topologies with N=4 are simulated by the microwave office program to achieve gain $|S_{21}| > 27$ dB over a bandwidth of 15 GHz with $g_m=0.05$, $Z_I=60 \Omega$, LI=0.4 nH, Cgs=0.08 pf, Cds=0.02 pf, and Cdg= 0.03 pf. The results are presented in **Fig.(5)** and (6). It can be observed that the proposed CSCSDA topology achieves the full bandwidth while the old CSSDA has about 3:1 reduction in the bandwidth as a result of Miller's effect. On the other hand, the return losses S_{11} and S_{22} of the new method are lower than those obtained by the old method.



Figure (4) 4-Stage CSCSDA



Figure (5) S-Parameters of 4-Stage CSSDA



Figure (6) S-Parameters of 4-Stage CSCSDA

5. Conclusion

This paper proposes a new topology for RF amplifier design. It achieves a considerable enhancement to the bandwidth of the conventional distributed amplifier by using cascode cells in the different amplifier stages.

The cascode eliminates the bandwidth degradation due to the Miller capacitance of the common-source stage's gate-drain capacitance. This degradation is particularly significant in CMOS circuits, where the gate-drain capacitance can be as high as one-third of the gate-source capacitance.

6. References

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