Simulation of Resistance Modulation in MOSFETs

Asst. Prof. Dr. Mohammed A. Abdala
College of Information Engineering
Nahrain University, Baghdad, Iraq

Abstract

Simulation results for the resistance modulation in metal-semiconductor field effect transistors (MOSFETs) are presented. The numerical simulations show that the resistance fluctuation does increase as the trap area is reduced, passes through a maximum and finally decrease towards zero.

The comparison of the simulated results with typical experimental Random Telegraph Signal (RTS) data shows an overall good agreement.

الخلاصـــــة

النتائج التحليلية للمعادلات الخاصة بحساب مقدار التغير في قيمة المقاومة لترانزستور تأثيري المجال نوع (MOSFET) تم عرضها في هذا البحث. إن النتائج التحليلية أظهرت زيادة في مقدار التغير في المقاومة مع تقليل مساحة الشوائب في المنطقة الفعالة، بعدها يصل مقدار التغير في المقاومة إلى قيمة عظمى وأخيراً يقل إلى أن يصل إلى الصفر. أن مقارنة النتائج التحليلية (RTS) مع النتائج العملية المتوفرة تبين توافق جيد بينهما.

1. Introduction

The occurrence of Random Telegraph Signal (RTS) in small area metal-semiconductor field effect transistors (MOSFETs) is generally attributed to individual carrier trapping at the Si-SiO_2 interface [1]. In a previous work [2], a theoretical analysis for the calculation of the resistance fluctuation in MOS devices have been introduced based on the assumption that the trap region in the channel of the device can be approximated by a rectangular region, and applying flat-band voltage and mobility fluctuations.

In this paper, the typical simulation results obtained from this model is presented and finally discussed with respect to typical experimental RTS data.

2. Theoretical Model

The normalized channel conductance fluctuation ($\Delta g_d / g_d$) and resistance fluctuation ($\Delta R_d / R_d$) is given by [2]:

$$\frac{\Delta R_d}{R_d} = \frac{\Delta g_d}{g_d} = \frac{\Delta w \Delta l \Delta \sigma}{w(l\sigma - \Delta l \Delta \sigma)} \quad \text{..... (1)}$$

where: Δw and Δl are the trap region dimensions while the channel has a width (w) and a length (l). $\Delta\sigma = (\sigma - \sigma)$ is the change in sheet conductivity, (σ_o) the sheet conductivity in the channel outside the trap region, and (σ) the sheet conductivity inside the trap region. For small modulation of conductivity ($(\Delta\sigma/\sigma) << 1$) and short trap region, ($(\Delta l / l) << l$), then the resistance fluctuation become:

$$\frac{\Delta R_d}{R_d} \approx \frac{\Delta w}{w} . \frac{\Delta l}{l} . \frac{\Delta \sigma}{\sigma} \quad \text{..... (2)}$$

And the flat band voltage in the region (V_{FB}) is given by:

$$V_{FB} = V_{FBO} - \frac{q}{\Delta w \Delta l C_{ox}} (l - \frac{d}{t_{ox}}) \quad \text{..... (3)}$$

where: (V_{Fbo}) is the flat band voltage outside the trap region, (d) the distance of the trap to the Si-SiO_2 interface, (t_{ox}) the gate oxide thickness, and (C_{ox}) the gate oxide capacitance per unit area.

For small conductance fluctuation amplitudes, the normalized sheet conductivity fluctuation can be given as:

$$\frac{\Delta\sigma}{\sigma} \approx \frac{\Delta\sigma}{\sigma_o} = -\frac{g_m}{I_D}\Delta V_{FB} = \frac{g_m}{I_D}\frac{q\left(1-\frac{d}{t_{ox}}\right)}{\Delta w \Delta l C_{ox}} \quad \text{..... (4)}$$

where: (I_D) is the drain current and (gm) the transconductance. Combining eq.(2) and (4) gives a first-order relation:

$$\frac{\Delta R_d}{R_d} = \frac{g_m}{I_D}\frac{q}{wlC_{ox}}\left(l-\frac{d}{t_{ox}}\right) \quad \text{..... (5)}$$

If the mobility (μ) dependence on oxide charge is taken account, then:

$$\frac{\Delta\sigma}{\sigma} = \frac{g_m}{I_D}\frac{q}{\Delta w \Delta l C_{ox}}\left(1-\frac{d}{t_{ox}}\right)\left(1 \pm \alpha\pi C_{ox}\frac{I_D}{g_m}\right) \quad \text{..... (6)}$$

where: (α) is a scattering constant (= 10^4 Vs/C), and the sign is chosen positive or negative for hole-like or electron-like traps respectively.

At strong inversion, the sheet conductivity fluctuation can be expressed in terms of the sheet concentration (N_s) as:

$$\frac{\Delta\sigma}{\sigma_o} = \frac{1}{\Delta w \Delta l N_s}\left(1 \pm \alpha\mu_o\frac{N_s}{q}\right) \quad \text{..... (7)}$$

where: μ_o the low field mobility.

In the weak inversion region, the resistance fluctuation can be given by:

$$\frac{\Delta R_d}{R_d} = \frac{\Delta w \Delta l(\gamma - 1)}{w(l\gamma - \Delta l(\gamma - 1))} \quad \text{..... (8)}$$

where: $\gamma = \exp(-\beta\Delta V_{FB})$, $\beta = \frac{q}{KT}\frac{C_{ox}}{(C_{ox}+C_d+C_s)}$, C_d the depletion region capacitance, C_s the oxide-semiconductor interfaces capacitance and (kT/q) the thermal voltage.

In the case of electron trapping in n-channel devices, and for large enough flat band voltage shift ($\Delta V_{FB} >> 1/\beta$), the resistance fluctuation reaches a limit given by:

$$\frac{\Delta R_d}{R_d} \approx \frac{\Delta w}{w} \quad \text{..... (9)}$$

Therefore, a maximum fluctuation of 100% may be reached when (i.e. trap region width = channel width). The same result is valid for whole trapping in p-channel device.

3. Model Simulation Results

The simulation result obtained using the model described in section (2) is presented in this section. The sheet conductivities in the channel outside and inside the trap region have been calculated using an analytical MOS transistor model [3]. This model outputs the corresponding inversion charge and mobility (therefore the sheet conductivity) for a creation given parameters such as the substrate doping (N_{sub}), the gate-oxide thickness (t_{ox}), and the flat band voltages outside and inside the trap region (V_{FBO} and V_{FB}). For these simulations, the parameters used were $N_{sub} = 10^{16}$ cm^{-3} (p-type substrate), t_{ox} = 25 nm, d = 0, π_o = 600 cm^2/V.S, 0=0.088 V, V_{FBo} = -0.6V and V_D = 50 mV. The effect of temperature was accounted for using classical Boltzmann statistics.

The resulting conductance fluctuation was then calculated using equations (1) and (3) as functions of gate voltage (VGS) for various channel dimensions, trap region size, and temperature. It is an analytical solution, how can you distinguish between both you have to explain.

The simulation results have also been compared with those given by the analytical models for weak inversion (equation (8)) and the small conductance fluctuation amplitudes (1^{st} order equations (5) and (6)).

3-1 Variation of Device Area

The variation of channel area can influence the amplitude of conductance fluctuation ($\Delta g_d / g_d$). This has been studied using equations (1) and (3) assuming mobility fluctuation to be negligible ($i.e\ \alpha = 0$). **Figure (1)** shows the simulated results of ($\Delta g_d / g_d$) as a function of drain current (I_D) for various device areas with a trap spread over the whole channel (*i.e* $(\Delta w/w) = (\Delta l/l) = 100\%$). In addition, the first order analytical model (using eq.(5)) is used to calculate ($\Delta g_d / g_d$) versus I_D and plotted on the same figure.

A good agreement between the simulation model and analytical model can be noted from **Fig.(2)**. This agreement is mainly due to the large size of the trap region used in the example (more than 10000 nm^2). It can also be noted that the relative conductance fluctuation is maximum at weak inversion (small I_D values) and then decreases as the device is drive into strong inversion (higher I_D values) in agreement with experimental data [4]. The analytical model (eq.(5)) shows a similar behavior due to the decrease of (g_m/I_D) with (V_G) and therefore with (I_D) [5]. Figure (1) also shows that the scaling down of the device produces an increase of the conductance fluctuation in accordance with theory (eq.(5)).

The influence of the constant trap area (400 nm_2) in which case equation (9) can be applied (very small trap area so that $\sigma << \sigma_o$) especially at weak inversion. Therefore, as

expected from eq.(9), the maximum conductance fluctuation obtained in weak inversion equals the ratio $((\Delta g_d / g)_{max})$, resulting in 20, 10, and 5% fluctuations for device of $(100)^2$, $(200)^2$ and $(400)^2$ nm^2, respectively.

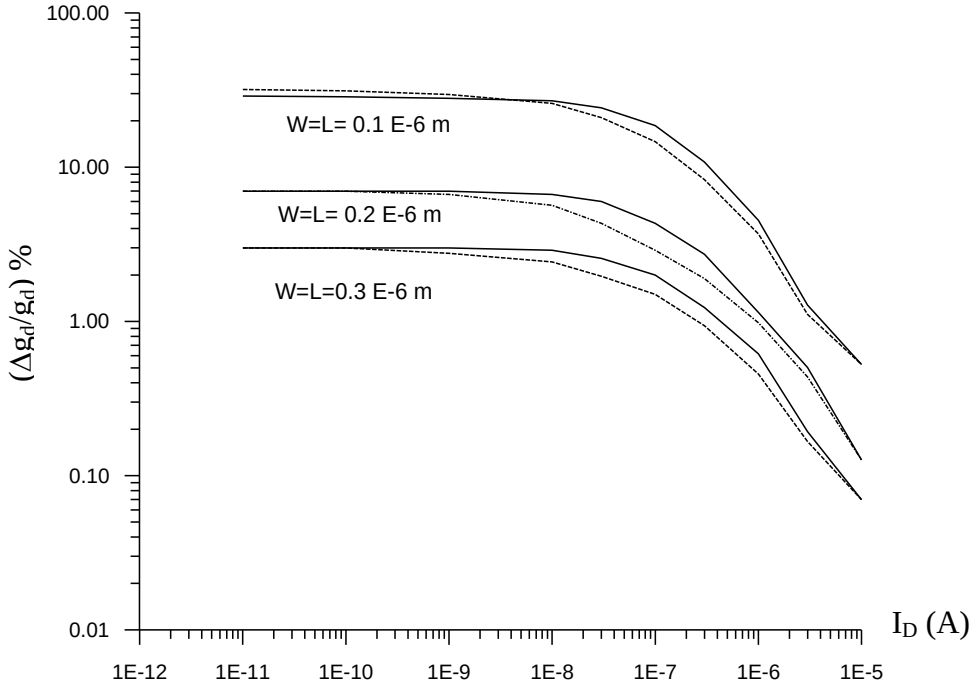

Figure (1) Simulated variation of ($\Delta g_d/g_d$) with I_d for various channel size w and l ($\Delta w/w = \Delta l/l = 100\%$)

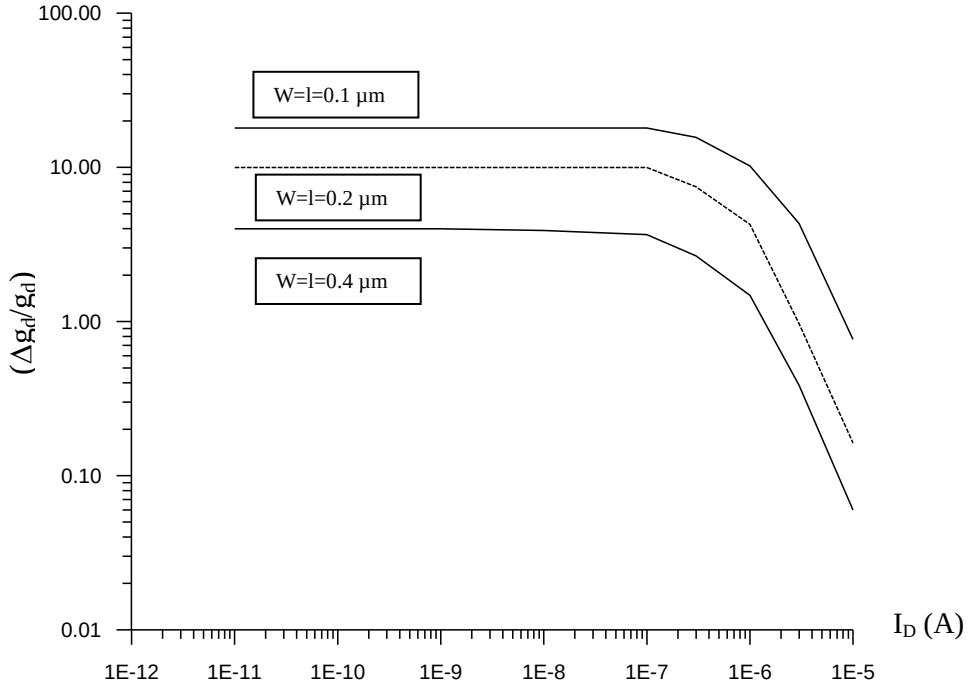

Figure (2) Simulated variation of (∆gd/gd) with Id for various channel size (w and l) with a constant trap area (400 nm2)

3-2 Variation of Trap Area

The analysis of the influence of the trap area for a constant device area is considered in this section. **Figure (3)** shows the conductance fluctuation variation with drain current for variation trap areas (as percentage of the device area). The figure shows that the maximum conductance fluctuation $(\Delta g_d / g)_{max}$ has a complex variation with the trap area. This can be easily seen in **Fig.(4)** in which $(\Delta g_d / g)_{max}$ has been plotted as a function of the trap region size. As predicted from the model (eq.(8)), it is clear that for not too small trap area, the conductance fluctuation is independent of trap region size. Reducing the trap region size makes the conductance fluctuation reach a maximum before decreasing to zero as $(\Delta w / w)$. **Figure (3)** also shows that for a small enough trap area the region of drain current over which $(\Delta g_d / g_d)$ is maximum extends more and more to the strong inversion region while the trap region size is decreases. This can easily be seen in **Fig.(5)** where $(\Delta g_d / g_d)$ is plotted against the gate voltage (V_{GS}).

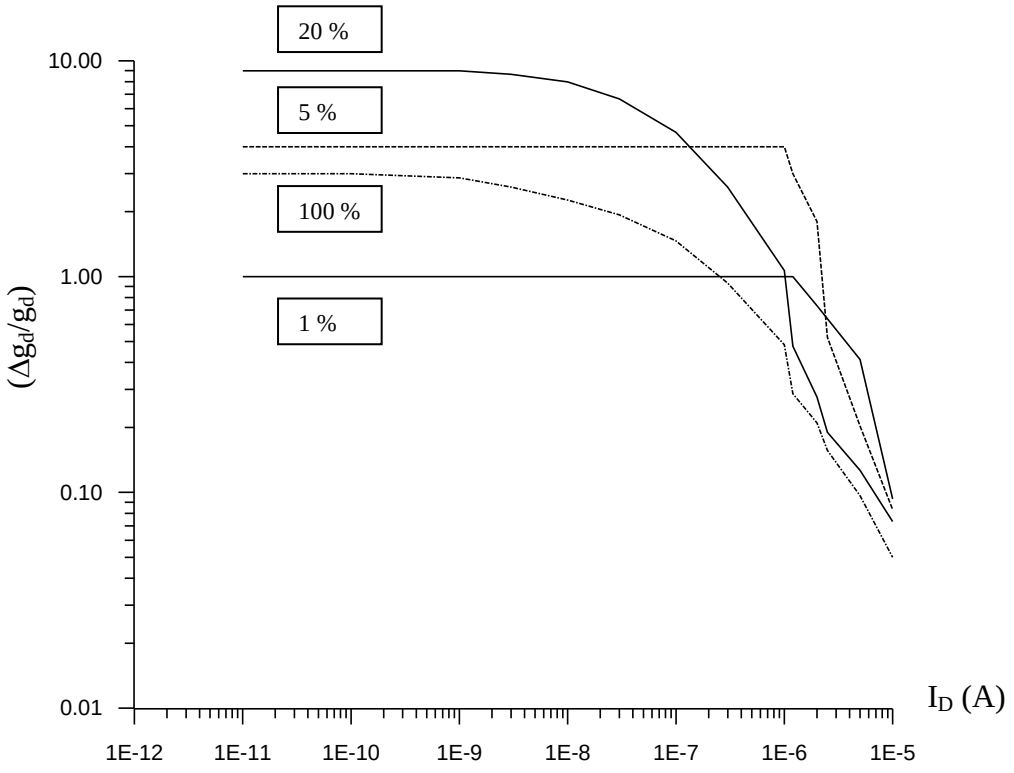

Figure (3) Simulated variation of $(\Delta g_d/g_d)$ with I_d for various trap size ($\Delta w/w = \Delta l/l$) (in %) at constant device area (w = l = 0.3 μm)

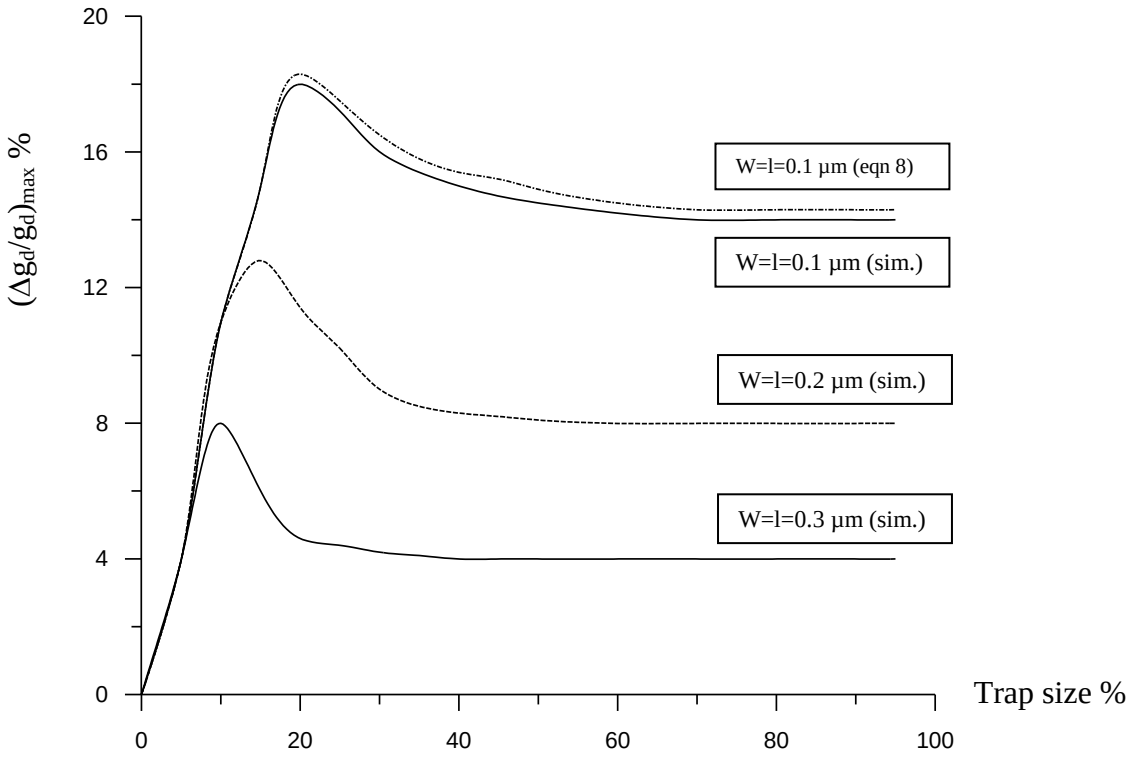

Figure (4) Simulated variation of the maximum $(\Delta g_d/g_d)_{max}$ with the size of trap region ($\Delta w/w = \Delta l/l$) (in percentage of device area) for various device areas

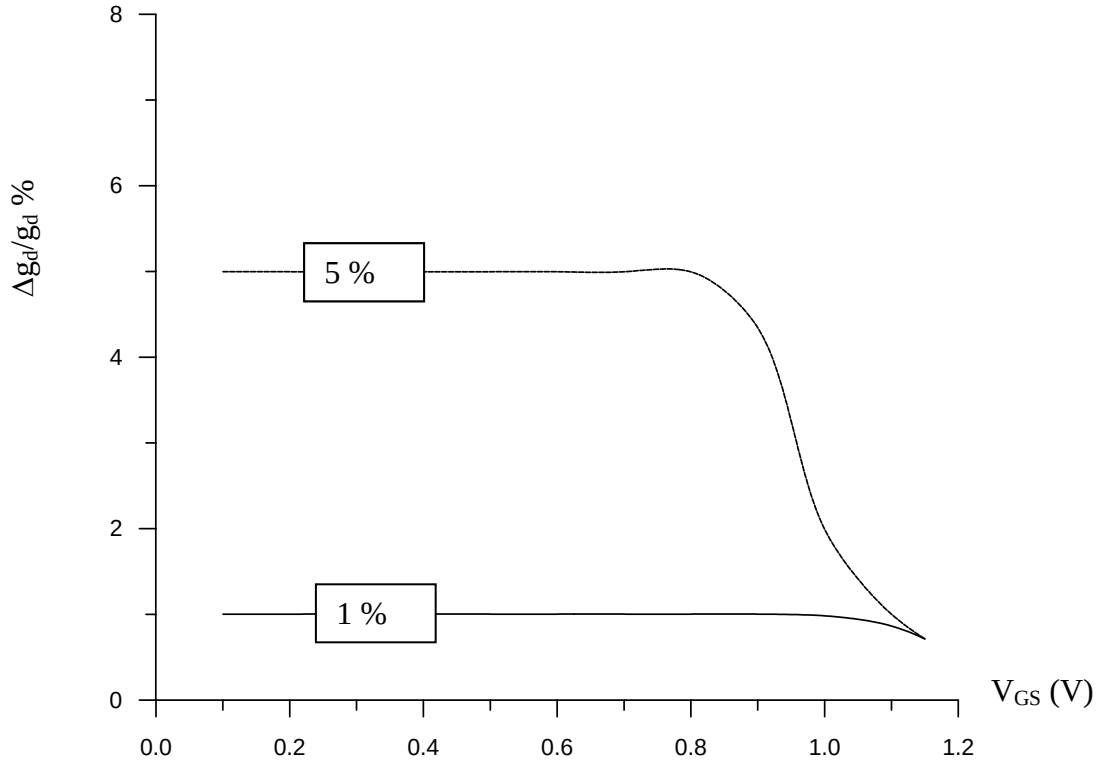

Figure (5) Simulated variation of (∆gd/gd) with gate voltage (VGS) for various trap sizes in a constant device area (w = l = 0.3 µm)

3-3 Variation of Mobility Fluctuation ($\alpha \neq 0$)

In this section, a study of mobility fluctuation due to its dependent on oxide charge is carried out. **Figure (6)** shows a comparison of ($\Delta g_d / g_d$) variation with scattering constant (α) for two cases with ($\alpha = 10^4 V_s / C$) and without ($\alpha = 0$) consideration of the extra mobility fluctuations. Therefore first-order analysis expects a discrepancy at strong inversion only [2]. This can easily be shown in **Fig.(6)** it is better to plot the inversion of conductance fluctuation ($g_d / \Delta g_d$) as a function of (V_{GS}) as shown in **Fig.(7)**. This figure shows that the absence of mobility fluctuation ($\alpha = 0$) leads to a linear variation of ($g_d / \Delta g_d$) with (V_{GS}), while in the presence of mobility fluctuation ($g_d / \Delta g_d$) varies nonlinearly with (V_{GS}) until it reaches saturation.

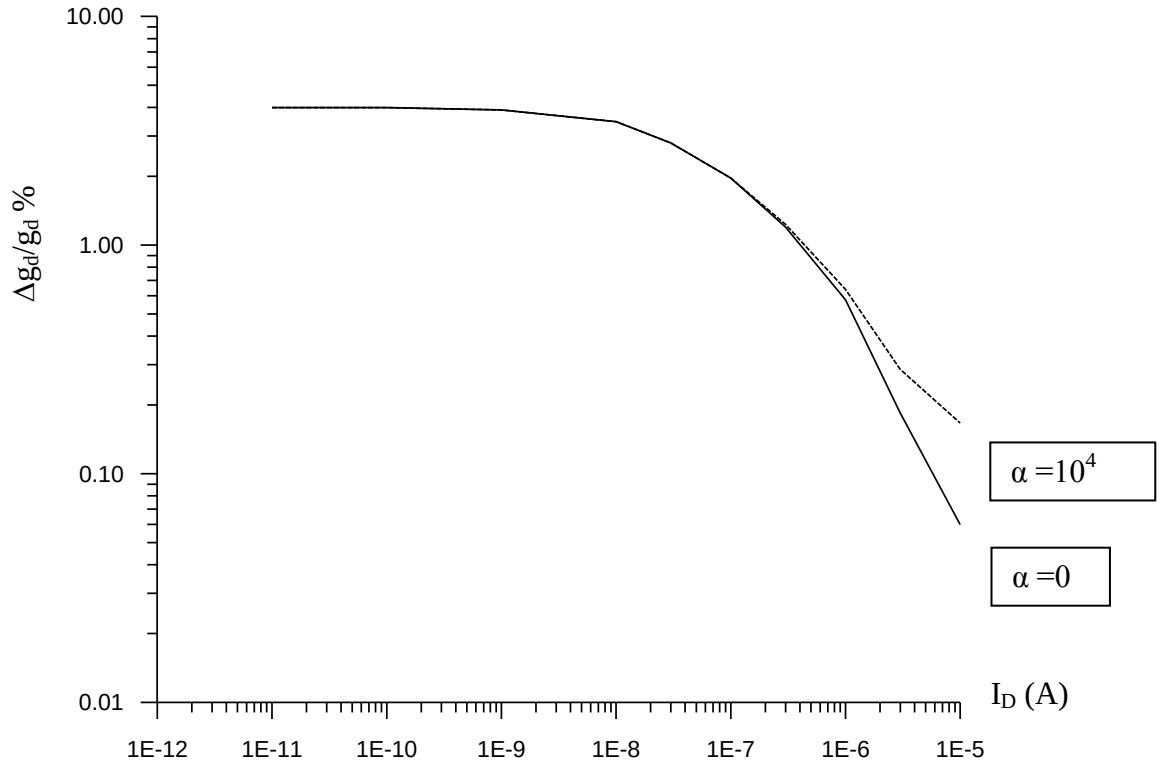

Figure (6) Simulated variation of ($\Delta g_d/g_d$) with I_d for (α=0) and ($\alpha = 10^4$ Vs/C) Device size (w = l = 0.3 μm) and trap area 100% of device

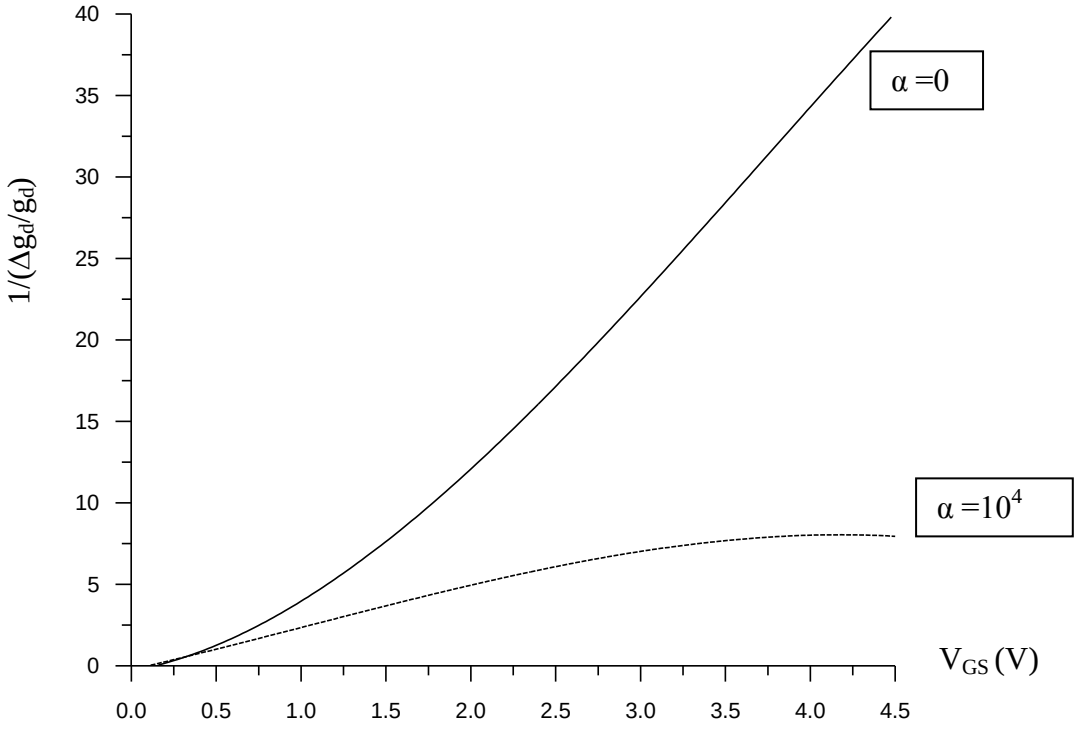

Figure (7) Simulated variation of (∆gd/gd) with Id for (α=0) and (α = 104 Vs/C) Device size (w = l = 0.3 μm) and trap area 100% of device

3-4 Variation of Temperature

The effect of temperature on the conductance fluctuation may be understood through eqs.(5) and (8). Equation (5) shows that the conductance fluctuation amplitude in weak inversion may vary as the inverse of temperature (T), since (g_m/I_d) α (q/kT). In addition, eq.(8) clearly shows that the effect of temperature should be maximized at low temperature. **Figure (8)** shows the maximum conductance fluctuation $(\Delta g_d / g_d)_{max}$ for various trap region size at a constant device area ($0.09\,\mu m^2$). This figure shows that, for a large trap region (100% of device area) and according to eq.(5), $((\Delta g_d / g_d)_{max}$ increase as the temperature decreases and could be saturated to 100% at low enough temperature. For smaller trap region sizes, $((\Delta g_d / g_d)_{max}$ reaches the maximum limit $(\Delta w / w)$ at higher temperature in the device with the smallest trap area.

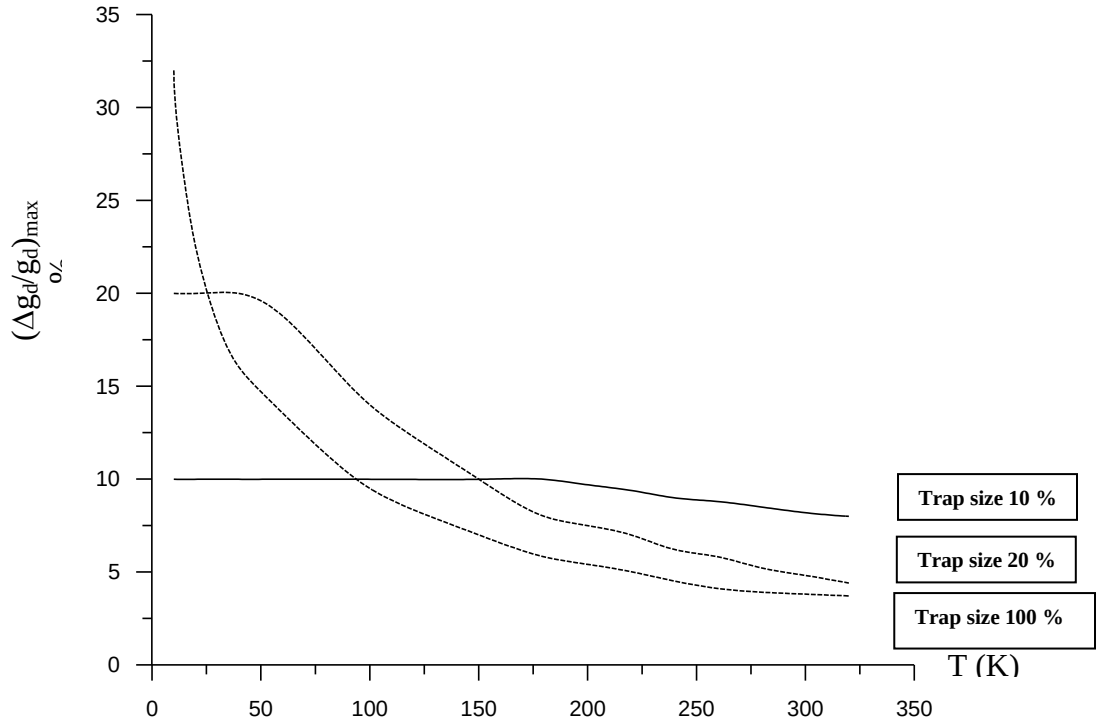

Figure (8) Simulated variation of the maximum $(\Delta g_d/g_d)_{max}$ with temperature (T) for various trap region sizes (in % of device area) in a device of dimension (w = l = 0.3 μm)

4. Comparison with Experiment

The simulation results are tested with respect to typical RTS experiment data given by other researchers. These data are mainly correspond to drain current fluctuation amplitudes as a function of drain current on a range which covers weak to strong inversion regions [4,6]. **Figure (9)** shows a curve fitting obtained when applying the model to the RTS data reported in references [4]. An overall good agreement between the model and the different kinds of the data (which corresponds to different samples) can be satisfied when varying the trap area. Particularly, the application of eq.(9) shows the constant amplitudes of the two smaller may in this case correspond to trap sizes around (2) to (2.5) nm.

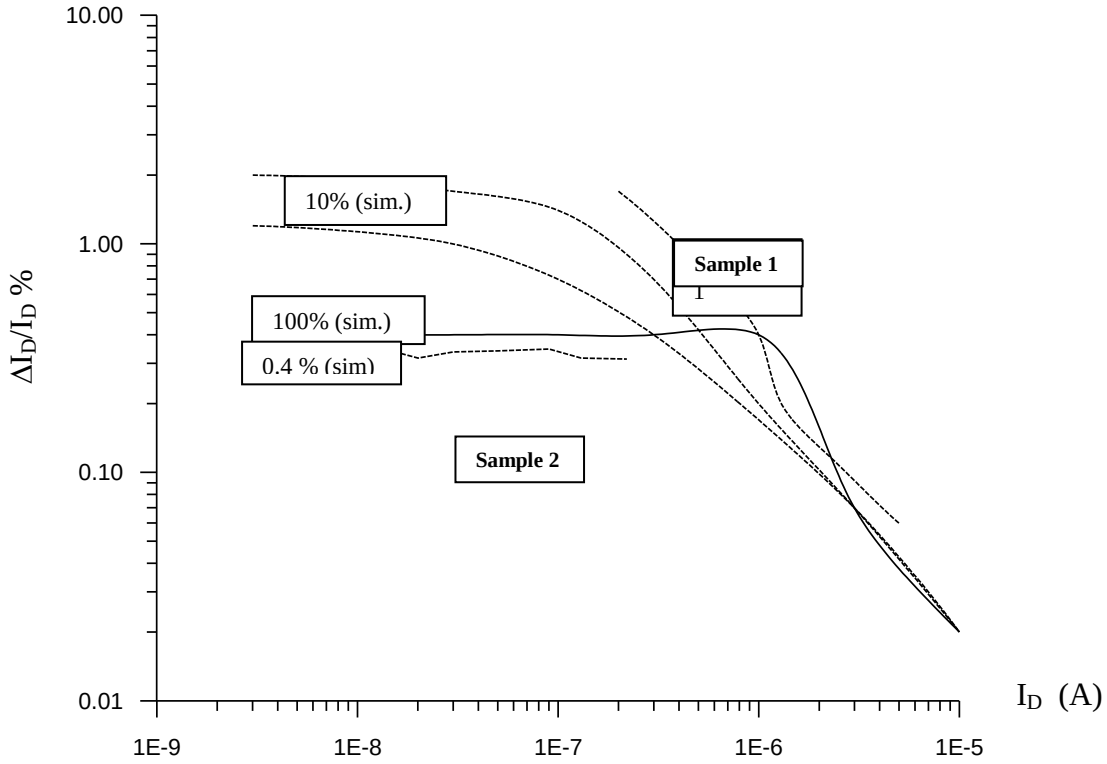

Figure (9) Typical experimental RTS amplitudes versus I_D (after ref [4] for two different samples) and corresponding simulated (fitted) obtained using our model

5. Conclusion

Simulation results have been used to show the effect of the trap area, device area, temperature, and the mobility correlated fluctuations on the conductance amplitude as a function of the drain current or gate voltage in ohmic operation. It has been found that the maximum RTS amplitude occurring in the size. However, the normalized conductance fluctuation does increase as the trap area is reduced, passes through a maximum, and then decreases towards zero. The comparison of simulation results with typical experimental RTS data shows an overall good agreement.

6. References

1. K., Ralls, W., Skocpol, L., Jackel, R., Howard, L., Fetter, R., Epworth and D., Tennat, ***"Discrete Resistance Switching in Sub-Micrometer Silicon Inversion Layers: Individual Interface Trap and 1/f Noise"***, Phys. Rev. Letters, Vol. 52, 1984, 228 p.

2. M., Abdala, "Resistance Modulation in MOSFETs", Proc. of the MCE 3rd Eng. Sci. Conf., 2000, 173 pp.

3. G., Ghibaudo, Phys. Stat. Sol. (a), Vol. 95, 1986, 323 pp.

4. M., Uren, D., Day, and M., Kirton, "1/f and Random Telegraph Noise in Silicon MOSFETs", Applied Phys. Letters, Vol. 47, 1985, 1195 pp.

5. G., Ghibaudo, ***"A Single Derivation of the Kubo-Greenwood Formula"***, Phys. Stat. Sol. (a), Vol. 113, 1989, 223 pp.

6. M., Kirton, and M., Uren, ***"Individual Interface State and their Implications for Low Frequency Noise in MOSFETs"***, Advance Physics, Vol. 38, 1989, 367 pp.