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ANALYSIS and SIMULATION of MOSFET DIFFERENTIAL AMPLIFIER

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Abstract: With the evolution of electronics today, a MOSFET transistor is useful in many applications such as computers due to several advantages. In this research, an NMOS transistor differential amplifier circuit with passive load that uses a modified Wilson current mirror as a biasing circuit is analyzed, designed and implemented. The width-to-length ratios of transistors are calculated by considering the voltage and current values at the output of the biasing circuit, and parameters such as conduction parameter, base width modulation parameter, and threshold voltage. A MATLAB version 8.1.0.604(R2010a) programming tool is employed for calculations and the simulations are carried out via Multisim 9 software tool. The output resistance obtained for current mirror is 2.297 MΩ. CMRR, output resistance, and power dissipation for differential amplifier circuit are 33.351 dB, 61.274 kΩ and 6.66 mW, respectively. The results show that the width-to-length ratio, differential gain and common mode rejection ratio are decreased with decreasing applied voltage at the output of the biasing circuit while approximately same values obtained for output resistance and common mode gain. The results show a good agreement between the measured values from simulation and the calculated one from design.

Key Words: *NMOS Transistor, Current Mirror, Differential Pair, Common Mode Rejection Ratio*

تحليل ومحاكاة المضخم التفاضلي الذي يستخدم الترانزستور المجالي نوع معدن- اوكسيد- شبه موصل

الخلاصة: مع تطور الالكترونيات في يومنا هذا، يعتبر الترانسستورالمجالي نوع معدن- أوكسيد- شبه موصل مفيد في كثير من التطبيقات مثل الحواسيب لمزاياه المتعددة. في هذا البحث، تم تحليل وتصميم وتنفيذ دائرة المضخم التفاضلي مع الحمل الخامل، ذات الترانسستور معدن- أوكسيد- شبه موصل النوع السالب، والتي تستعمل دائرة مراة التيار Wilson المعدلة كدائرة انحياز. تم حساب نسبة العرض-الى-الطول لجميع الترانسستورات عن طريق أعتبار قيم الفولتيات والتيارات عند خرج دائرة الانحياز اولا والمتغيرات مثل متغيرالتوصيل ومتغير تعديل عرض القاعدة وفولتية العتبة. استخدمت الاداة البرمجية MATLAB version 8.1.0.604(R2010a) لغرض الحسابات واما المحاكاة فتمت عبر الاداة البرمجية Multisim 9. أن القيمة المستحصلة لمقاومة الخرج دائرة مراة التيار 2.297 MΩ. اما في دائرة المضخم التفاضلي فكانت قيمة نسبة رفض الوضع المشترك 33.351 dB ومقاومة الخرج 61.274 kΩ واستهلاك القدرة فهو بحدود 6.66 mW على التوالي. أظهرت النتائج نقصان نسبة العرض-الى-الطول لترانسستورات الزوج التفاضلي وكذلك نقصان كل من الكسب التفاضلي ونسبة رفض الوضع المشترك مع نقصان الفولتية المطبقة عند خرج دائرة الانحياز مع تقريبا بقاء نفس القيم لكل من مقاومة الخرج وكسب الوضع المشترك. أظهرت النتائج أن القيم المقاسة من دائرة التنفيذ في أتفاق جيد مع القيم المستحصلة من الحسابات.

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1. Introduction

In integrated circuits, p- and n-types MOS (metal-oxide-semiconductor) current mirrors can be used as biasing and active load circuits. This circuit consists of a diode-

connected and perfectly matched transistors operated in saturation, and also at same temperature. A reference current is injected in the input and the output current is taken from the output of the mirror [1-3].

Different values of these currents can be obtained by designing width-to-length ratio, (W/L), of the MOS transistors. A high output resistance is an important parameter for these circuits; a value of 4.5 MΩ [4] is obtained for modified Wilson current mirror. The differential amplifier is an extremely common circuit in integrated circuits. The MOS version of this circuit consists of two transistors biased by current source, the sources of these transistors are connected together and the drains are connected to two resistors as passive load. The resistors operate the transistors in saturation and the whole circuit is biased from a current provided by current mirror circuit. The power dissipation of this circuit is 6.04 mW [5]. Active load may replaces resistors by transistors and the differential amplifier then has both p- and n-types transistors, i.e. CMOS amplifier (C; stands for complementary) [6-7]. As known, the differential amplifier has two inputs and two outputs; signals can be applied at its inputs. The output signals are out-of-phase and the amplified voltage values at outputs are according to difference between the inputs. The circuit operates from two supplies or even one supply. For high performance, suitable differential amplifiers can be analyzed, designed, and simulated for numerous applications [8-9].

2. Biasing Circuit Design

An improved NMOS Wilson current mirror is used as shown in "Fig. 1", transistor T_1 is to provide reference current and the circuit is biased at ± 6 V.

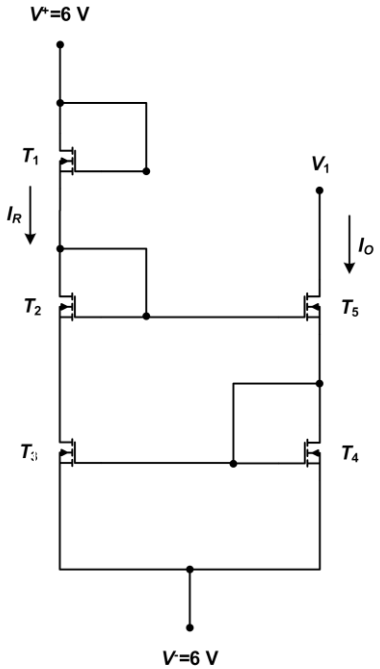

Figure 1. Biasing circuit.

The specified parameters for designing NMOS transistors are;

- Conduction parameter $k_n' = 80\ \mu\text{A/V}^2$
- Base width modulation parameter $\lambda_n = 0.02\ \text{V}^{-1}$
- Threshold voltage $V_T = 1$ V.

The biasing currents are;

- Reference current $I_R = 800\ \mu$A
- Output current $I_O = 812\ \mu$A

To calculate (W/L) for the transistors, consider first the voltage at the drain of T_5 to be $V_1 = 2$ V. Let the drain to source voltage of T_4 is $V_{DS5} = 4$ V, so

$$V_1 - V_{DS5} - V_{Ds4} + 6 = 0 \qquad (1)$$

$$V_{DS4} = 4\ \text{V}$$

Transistor T_4 is a diode-connected transistor so gate-to-source voltages are $V_{GS4} = 4$ V and $V_{GS3} = 4$ V for matched T_3 and T_4 transistors. The ratio of output and established reference current is given by [10]

$$\frac{I_O}{I_R} = \frac{1 + \lambda_n V_{DS4}}{1 + \lambda_n V_{DS3}} \qquad (2)$$

Using above values

$$\frac{812}{800} = \frac{1 + 0.02(4)}{1 + 0.02(V_{DS3})}$$

$$V_{DS3} = 3.202\ \text{V}.$$

Assuming that T_1 and T_2 are identical, so $V_{GS1} = V_{GS2} = V_{GS}$. From Kirchhoff's voltage law

$$V^+ - V_{GS1} - V_{Gs2} - V_{Ds3} + V^- = 0 \qquad (3)$$

$$6 - 2V_{GS} - 3.2 + 6 = 0$$

$$V_{GS1} = V_{GS2} = 4.399\ \text{V}$$

V_{GS5} is found from

$$V_{Ds3} + V_{GS2} - V_{Gs5} - V_{Gs4} = 0 \qquad (4)$$

$$V_{GS5} = 3.601\ \text{V}$$

The obtained voltages set all transistors in the saturation region, (W/L) for transistors can be calculated as;

i- For T_1 and T_2: $V_{GS1} = V_{GS2} = 4.399$ V and $V_{DS1} = V_{DS2} = 4.399$ V so (W/L) for these transistors are obtained from

$$I_{\mathrm{R}} = \frac{k_n'}{2}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2(1 + \lambda_n V_{DS}) \qquad (5)$$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 1.5911$$

ii- For T_3: $V_{GS3} = 4$ V and $V_{DS3} = 3.202$ V, from (5)

$$\left(\frac{W}{L}\right)_3 = 2.0885$$

iii- For T_4 and T_5, (W/L) is determined from

$$I_{\mathrm{O}} = \frac{k_n'}{2}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2(1 + \lambda_n V_{DS}) \qquad (6)$$

Since $V_{GS4} = 4$ V, $V_{DS4} = 4$ V, $V_{GS5} = 3.601$ V, and $V_{DS5} = 4$ V, so

$$\left(\frac{W}{L}\right)_4 = 2.0885$$

and

$$\left(\frac{W}{L}\right)_5 = 2.7783$$

The calculated values above are obtained from MATLAB programming tool version 8.1.0.604(R2010a) [11] according to the specified parameters for design. The biasing circuit with Multisim 9 [12] is simulated in "Fig. 2".

3. Differential Circuit Design

The differential amplifier circuit consists of ± 4 V supply at the gates of identical transistors T_6 and T_7, and two load resistors of 5.1 kΩ each shown in Fig. 3. The differential pair is biased by constant current source I_O that is divided equally between T_6 and T_7. The quiescent current in each of load resistors is the given by

$$I_{DQ} = \frac{I_O}{2} = 406\ \mu\mathrm{A}$$

then voltages at load resistors is $V_R = 2.07$ V. The drain-to-source voltage at T_6 is given by

$$V_{DS6} = V^+ - V_R - V_1 \qquad (7)$$

hence $V_{DS6} = 1.93$ V and $V_{GS6} = 2$ V. From symmetry, the (W/L) ratio for T_6 and T_7, which they are biased in the saturation region, is found from (6) as

$$406 = \frac{80}{2}\left(\frac{W}{L}\right)(2-1)^2(1+(0.02)1.93)$$

$$\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_7 = 9.7729$$

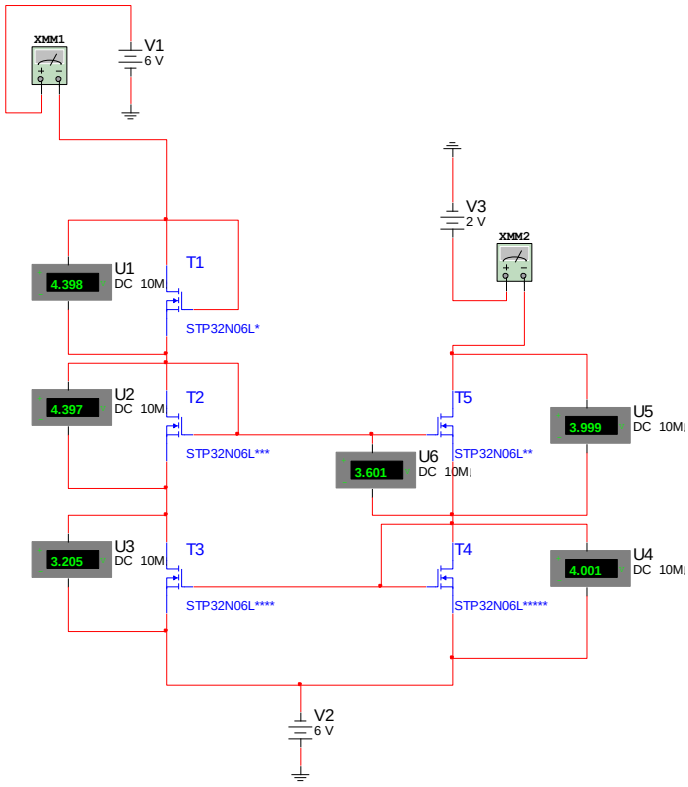

Figure 2. Biasing circuit simulation.

4. Differential Gain, Common Mode Gain, and Common mode Rejection Ratio

The differential-mode gain is [10]

$$A_d = \frac{g_m R}{2} \tag{8}$$

where g_m is the transconductance given by

$$g_m = 2\sqrt{\frac{k_n'}{2}\left(\frac{W}{L}\right)I_{DQ}} \tag{9}$$

Therefore $g_m = 1.1$ mA/V, and $A_d = 2.87$. The common-mode gain is

$$A_C = \frac{-g_m R}{1 + 2g_m R_O} \tag{10}$$

where R_O is the output resistance given by

$$R_O = \frac{1}{\lambda_n I_O} \tag{11}$$

so $R_O = 61.756\ \text{k}\Omega$, and $A_C = -0.0411$. and the common-mode rejection ratio, CMRR, is

$$\text{CMRR}=20\log\frac{A_d}{|A_C|} = 20\log\frac{2.87}{0.041} = 36.88\ \text{dB}$$

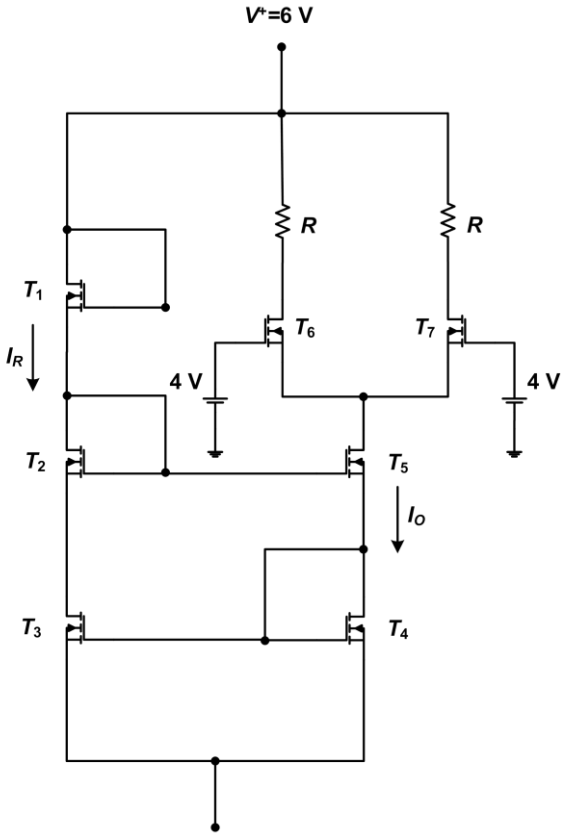

Figure 3. Differential amplifier circuit.

5. Results

The complete designed circuit values are also accomplished with MATLAB computer program and it is simulated as shown in "Fig. 4". In this circuit, STP32N0GL power NMOS transistor type is used, an input dc common-mode voltage of 4 V is applied to T_6 and T_7 for specifying V_{GS6} and V_{GS7}. The measured reference current is 804 μA and the current source transistor T_5 supplies a current of 816 μA. For the current mirror, the output resistance is 2.297 MΩ compared with 4.5 MΩ in [4]. For the differential-mode gain measurement, an input signal voltage of ± 4 mV is applied, this given in r.m.s values as 0.0028 V. The measured output signal voltage is about 16 mV,

so $A_d = 16/8 = 2$, for the common-mode gain measurement, an input of $+4$ mV is also applied, and the measured output voltage is about 173 μV, so $A_C = 0.173/4 = 0.043$, hence CMRR is 33.351 dB, and the output resistance is 61.274 kΩ. The power dissipation of the differential amplifier circuit is 6.66 mW compared with that of 6.02 mW [5]. The results obtained from simulation are in good agreement with the calculated values.

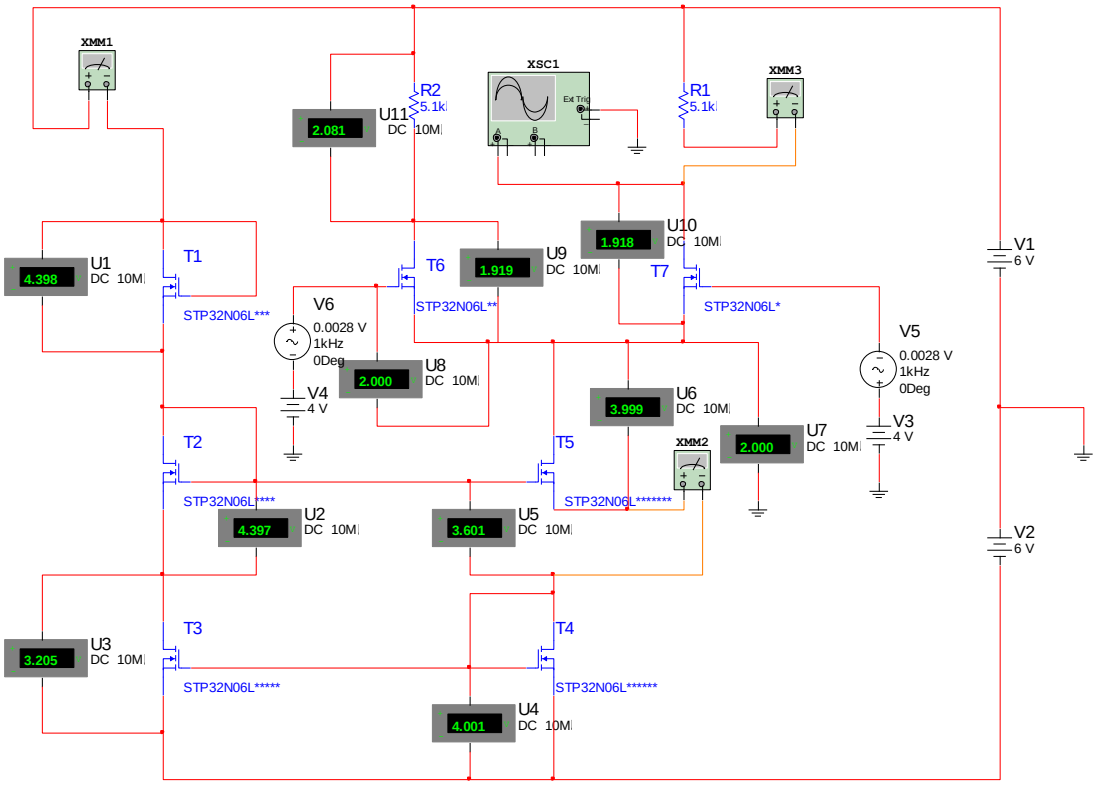

Figure 4. Designed circuit.

6. Discussions

The voltages in the circuit can be varied according to the changing of voltage values at the drain of transistor T_5, which is V_1, and changing I_O/I_R value to show the effect of I_O. So two cases are considered, the first, is illustrated in the first two rows of Tables. 1, 2, and 3. , for $V_1 = 2.5$ V and 1 V at $I_O/I_R = 812$ μA/800 μA. The second is shown in the third row of these tables for which $I_O/I_R = 612$ μA/600 μA at $V_1 = 2$ V. The (W/L) ratios for T_6 and T_7, the differential pair transistors, shown in Table. 2, is decreasing with decreasing V_1, this is due to decrease in gate-to-source voltages. Both the differential gain and the common mode rejection ratio are also decreasing, with decreasing in V_1, as shown in Table. 3, and this because of decreasing in the transconductance parameter which in turn related to (W/L) ratio. The output resistance and common mode gain are unchanged in this case. The values in the third row, are compared with the calculated values obtained from design. Approximately, same values obtained for (W/L) ratio, differential gain, and the common mode rejection ratio with a decrease in common mode gain when output current decreases, but the output resistance

is increased in this case due to inverse relation with output current. The amplified output voltages together with the input voltages obtained from the simulation process of the differential amplifier are shown in "Fig. 5", "Fig. 6", and "Fig. 7", respectively.

Table 1. Voltages Values of differential amplifier circuit.

V_1	V_{GS1}	V_{GS2}	V_{GS3}	V_{DS3}	V_{GS5}	V_{DS5}	V_{GS6}	V_{GS7}	V_{DS6}	V_{DS7}	V_{R1}	V_{R2}
2.5 V	4.152 V	4.152 V	4.5 V	3.696 V	3.348 V	4 V	1.5 V	1.5 V	1.419 V	1.419 V	2.081 V	2.081 V
1 V	4.89 V	4.889 V	3.002 V	2.222 V	4.108 V	4.019 V	2.979 V	2.979 V	2.899 V	2.899 V	2.08 V	2.08 V
2 V	4.441 V	4.44 V	4.001 V	3.119 V	3.558 V	3.999 V	1.999 V	1.999 V	2.433 V	2.433 V	1.556 V	1.556 V

Table 2. Width-to-length ratios of transistors' circuit.

V_1	$(W/L)_1$	$(W/L)_2$	$(W/L)_3$	$(W/L)_4$	$(W/L)_5$	$(W/L)_6$	$(W/L)_7$
2.5 V	1.8579	1.8579	1.5203	1.5203	3.4114	39.4716	39.4716
1 V	1.2029	1.2029	4.7877	4.7877	1.9454	2.3971	2.3971
2 V	1.1624	1.1624	1.5689	1.5689	2.159	7.2696	7.2696

Table 3. Performance parameters.

V_1	g_m	R_o	A_d	A_C	$CMRR$
2.5 V	0.0023	61.576 kΩ	5.774	0.0413	42.91
1 V	0.00055	61.576 kΩ	1.423	0.04	30.84
2 V	0.00084	81.967 kΩ	2.1479	0.0309	36.84

7. Conclusions

For MOS differential amplifier circuit, the biasing circuit considered is modified Wilson current mirror with four transistors architecture since this circuit provides an increase in the output resistance for better performance. The analysis of width-to-length ratio, common-mode gain, differential-mode gain, and common-mode rejection ratio are performed with MATLAB computer program version 8.1.0.604(R2010a). The circuit is implemented in Multisim 9. Both, a change in applied voltage at the output and a change in output current, for the biasing circuit affect the performance parameters. A better (W/L) ratio is obtained when the voltage at the output of biasing circuit is decreased but this cause a decrease in differential gain and the common mode rejection ratio. The output resistance for current mirror is 2.297 MΩ and it can be enhanced by decreasing the output current of the biasing circuit. For differential amplifier circuit, CMRR is 33.351 dB, output resistance is 61.274 kΩ, and power dissipation is 6.66 mW.

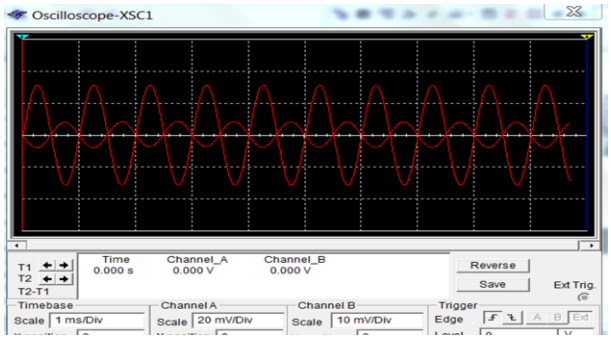

Figure 5. Output and input voltages of differential amplifier circuit at $V_1 = 2.5$ V.

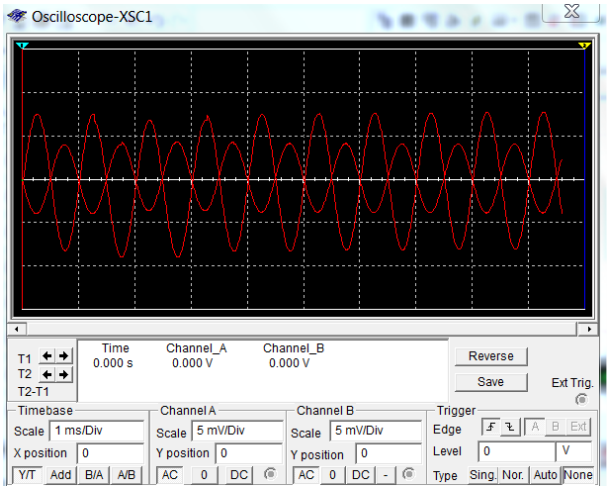

Figure 6. Output and input voltages of differential amplifier circuit at $V_1 = 1$ V.

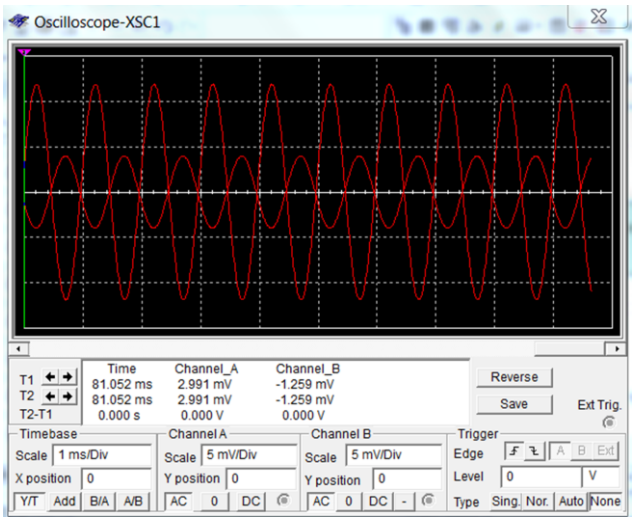

Figure 7. Output and input voltages of differential amplifier circuit at $V_1 = 2$ V, and $I_O/I_R = 612$ µA/600 µA.

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