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Text Coding Using FPGA Spartan-XL Electronic Platforms

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Abstract

The Field Programmable Gate Array (FPGA) approach is the most recent category, which takes the place in the implementation of most of the Digital Signal Processing (DSP) applications. It had proved the capability to handle such problems and supports all the necessary needs like scalability, speed, size, cost, and efficiency. In this paper a new proposed circuit design is implemented for text coding with an implemented example using FPGA is provided. In this implementation, the evaluations of the text coefficients are evaluated on the Scrambling – Coding, and the De-Scrambling - De-Coding sides. This implementation was achieved using an FPGA Kit after building the logical circuits on the specified kit that uses the Spartan-XL electronic library type implemented using the ISE-4.1 software which is one of the latest versions of the Xilinx Foundation Series 2.1I software.

الخلاصـــــة

أن خاصية الـ (FPGA) هي من أحدث الخواص و التقنيات التي تم تطويرها في مجال الدوائر الإلكترونية و التي دخلت في الكثير من المجالات العلمية خاصة في مجال معالجة الإشارات الرقمية.

لقد أثبتت هذة التقنية قابليتها عل تولي القيام بالكثير من الأعمال و دعم الكثير من أحتياجات بعض التطبيقات التخصصية و التي تحتاج الى الدقة و السرعة و الحجم و الكلفة.

في هذا البحث تم تصميم دائرة الكترونية الغرض منة تشفير النصوص المكتوبة و تنفيذها على دائرة مصنوعة من رقائق ألكترونية تعتمد الية الـ (FPGA) حيث تم بناء الدائرة و تنفيذها و تمت محاكاة التصميم من خلال مثال عملي تم تنفيذة على برنامج شركة (Xilinx) ذا الأصدار 2.1.

1. Introduction

Hiding, Scrambling, Encrypting, Coding…etc are the most important processes now a days since the type of wars is changed from the classical ones with bolts and guns to more effective and higher technology ones that uses informations and bits [1].These great changes lead to change the type of data securing that fits these changes by using highly secured, complicated, large speed processing systems in order to be able to have the best response for such purposes [2].

The Field Programmable Gate Array (FPGA) technology was the remedy that takes the place in the fast electronic devices society and it had proved its fitness for handling tasks specialized with very fast, accurate, complicated processes. Where these tasksimplemented with an exceptional efforts and costs. This lead to make these electronic kits are the new lead for a brand new branch in the designing of all digital systems specially the ones used in the security systems.

Text is the most important type of data since nearly 75% of secured data exchange is represented by messages which leads to make them as secured as possible specially secret and top – secret ones. Because the available amount of data in the text is less than the amount of data in the image or the voice and the needs for transmitting the text are less complicated that the other ones like the bit rate and the channel bandwidth [3,4].

In this paper a new design for a circuit that can perform the data scrambling and coding on the transmitting and receiving sides are dedicated. The circuit operates in a high speed (Operating frequency is 1GHz). Short processing time and high accuracy (32 bit for the data and five for control bit). Receiving data in many ways whether its serial or parallel and produce data in serial or parallel which made the circuit can be used for general purposes easily on both the transmitting and receiving sides.

2. Text Coding

One of the most important strategies for data hiding that is used in data security category is text coding. Since it's well known that each letter (capital or small or sign) has its own ASCII (American Standard Code for Information Interchange) code which consist of 7 bits which leads to have a sign letter out of 128 ones [5,6]. Therefore text coding depends upon the implemented text hiding functions inside the processing circuit because as much as the Coding function is complex its difficult to be broken. But at the same time it will be time consuming and in need for more arithmetic operations to handle the task which leads to make the circuit in need for more processing power (this means in need for more electric power and high-speed components with more complex circuit design)[5,7].

In this paper text, coding is first performed by changing the number of bits of each letter to a new number of bits that fits the system. Then the system proceeds to perform the coding process on the modified text. At the end of the process, the data will be ready to be transmitted. On the other side, the data must be Re-Processed in order to De-Code the data and then retrieve the original amount of bits per letter where the text data now are the same as the ones at the start of the process.

3. Demonstrated Example

In this system, the ASCII code of the text will be translated to a stream of bits. The ASCII code of each letter that consists of 7 bits will be manipulated to be 8 bits (lead to have a sign letter out of 256) where in spite of increasing the over all text size but this will reduce the probability of breaking the code. These bits will enter the processing circuit throw the Serial – In – Parallel – Out Shift register where the data will be coded and scrambled with a special processing circuit in order to hide the original text. Fig (1) & (3) shows the circuit designs in the transmitting & receiving sides. Fig (2) & (4) shows the circuit-timing diagram and the system output for the input applied to the circuit and the output of the circuit. Table (1) & (2) shows the bit stream response of the system from the bit entrance to their outlet at both sides.

4. FPGA Simulation of Text Coding Systems

This paper shows a new method for designing an FPGA digital circuit for the evaluation of the coefficients of Text Coding implemented using the ISE-4.1 software produced by Xilinx Company for FPGA electronic kit productions, which represents one of the most recent updates for the Xilinx Foundation Series 2.1i. Therefore, the simulation process should pass through four stages.[8]

The problem formulation and function establishment represents the first stage. The second stage is represented by over coming the limitations and difficulties in a reasonable way keeping an eye to the over all cost. Operating the optimized designed kit represents the third stage. The fourth stage is represented by connecting the designed kit to the operating environment and search for its compatibility and the best ways for operating in the presence of other system equipments.[9,10]

For the first stage, specifying the coding function represents the problem formulation where this function specifies the type of text processing and the way of increasing the number if bits from 7 bits to 8 bits. For the second stage, the FPGA kit for the implemented design is SPARTAN-XL .The SPARTAN-XL 1.8V FPGA gives high performance, abundant logic resources, rich features set, all at exceptional low price. This family contains seven members offers density range from 50000 to 600000 system gates with wide operating frequency range (500KHz – 2.5GhHz), delivering more I/Os and other features per dollar than other FPGAs by combining advanced process technology with a streamlined architecture based on the proven Vertex-E. Features include Block RAM (288 K bit), Distributed RAM (221K bit), 19 selectable I/O standard, 4 DLL (Delay Locked Loop), Fast Predictable Interconnection means that successive design iteration continue to meet timing requirements.[8,9]

The third stage depending upon the type of application, its operating frequency, its operating speed, and its response time. For example if we are dealing with speech signal then

the highest possible frequency component does not accede 6KHz in any way. And the speech rate is relatively slow; while in target identification the image verification must be real time and very accurate with a very high response speed for direction changing.[6,8]

Or if systems are not in need for high speed and have symmetry in their circuits architecture then these symmetric circuits can be combined in few ones and the operations may be performed in sequence, or else redundant circuits will be built to perform parallel processing or pipe lining to achieve the necessary operating speed. The fourth stage is represented by implementing the whole system from its receiving point to its transmitting point since the used kit is more than enough to handle this task from size, speed, accuracy, cost. So; building the whole system on the same kit reduces the compatibility problems to the minimum. [10]

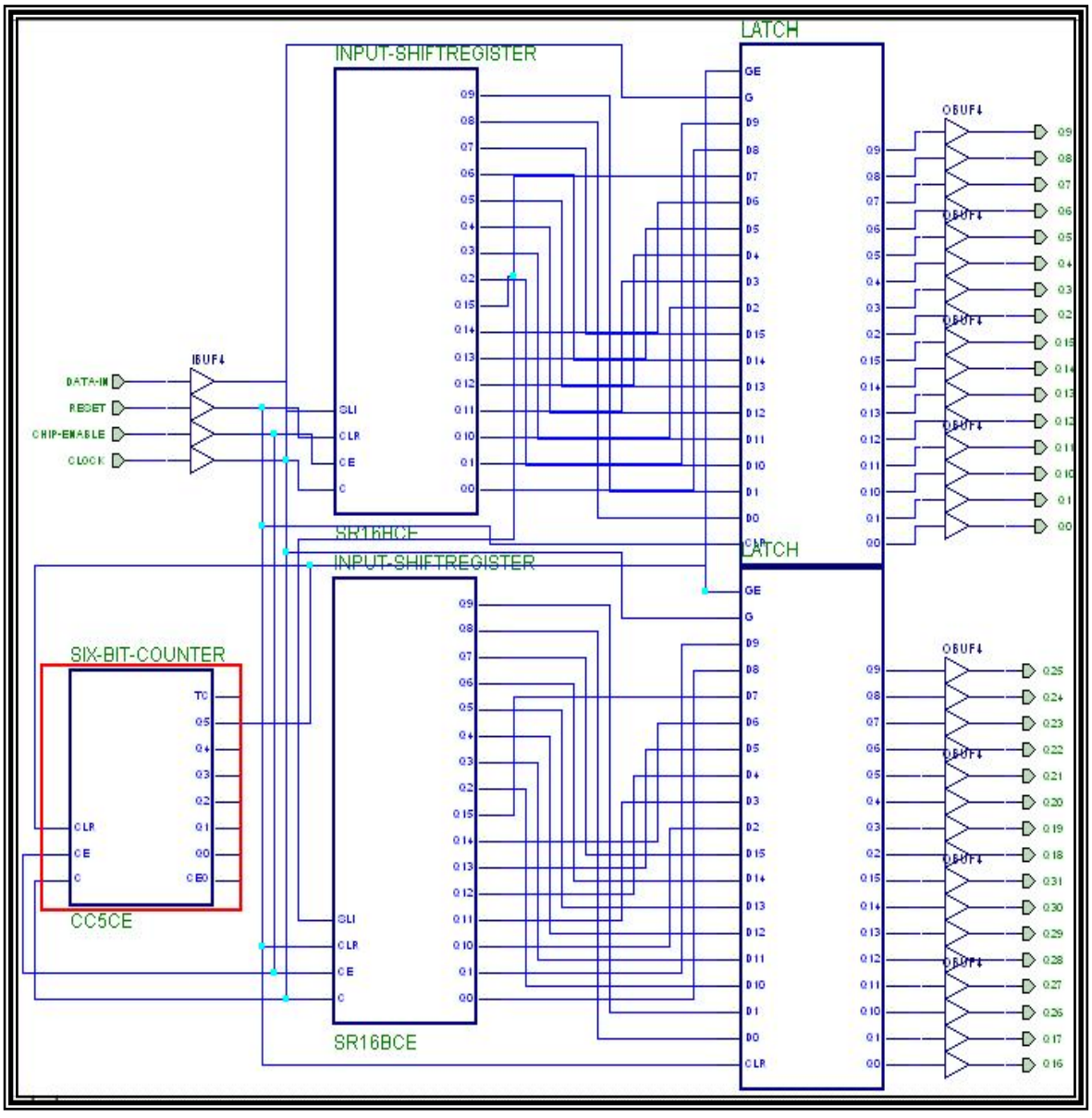

Fig (1): - The circuit design for text coding at the transmitting side

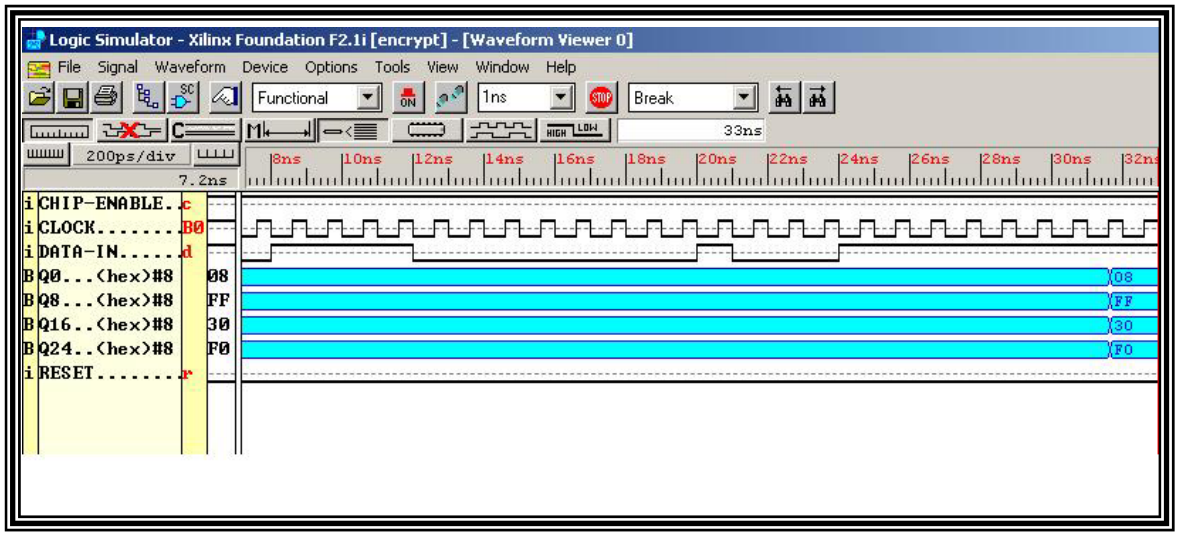

Fig (2): - Timing Diagram for the input and output data of the circuit

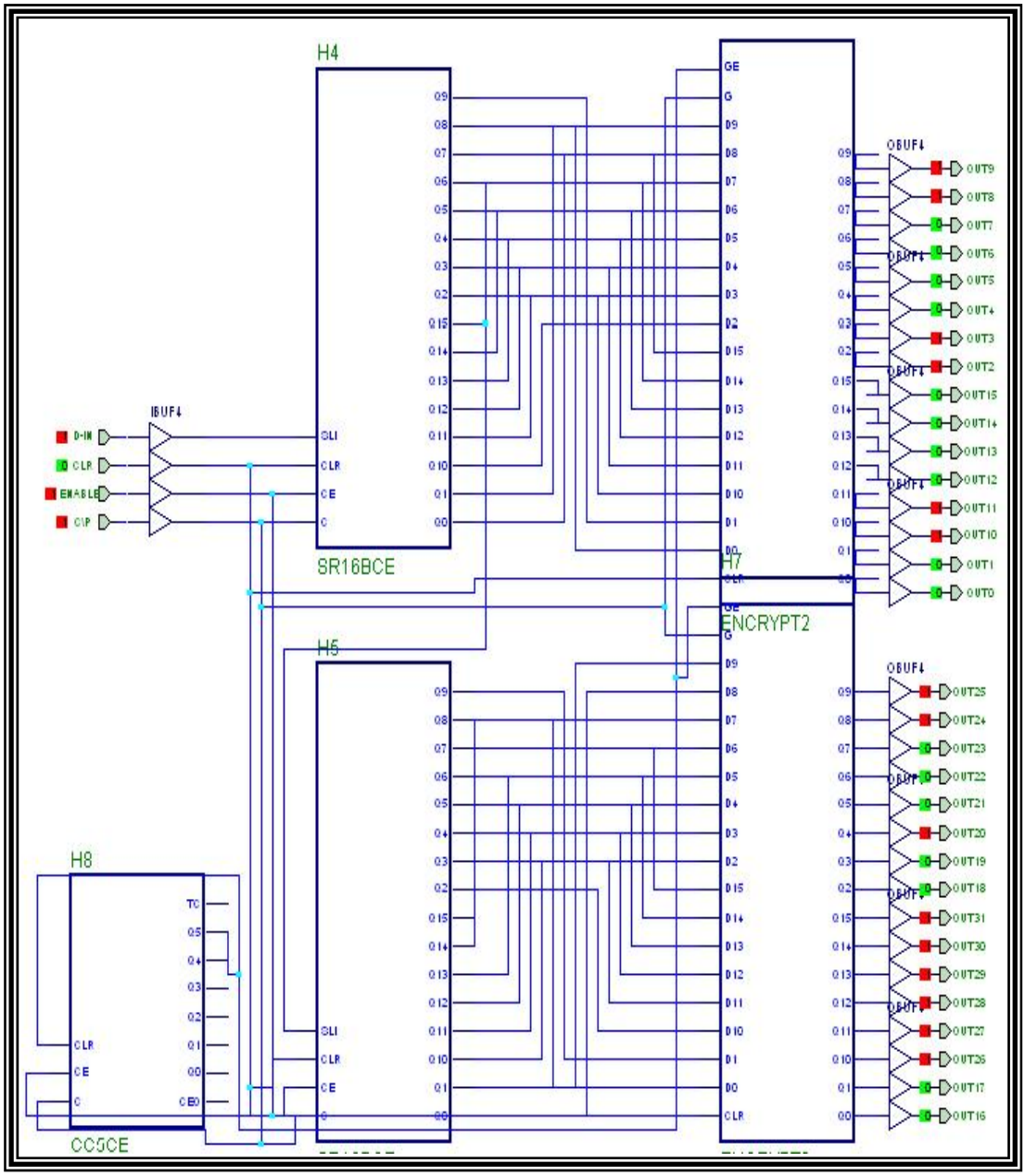

Fig (3): - The circuit design for text De-coding at the receiving side

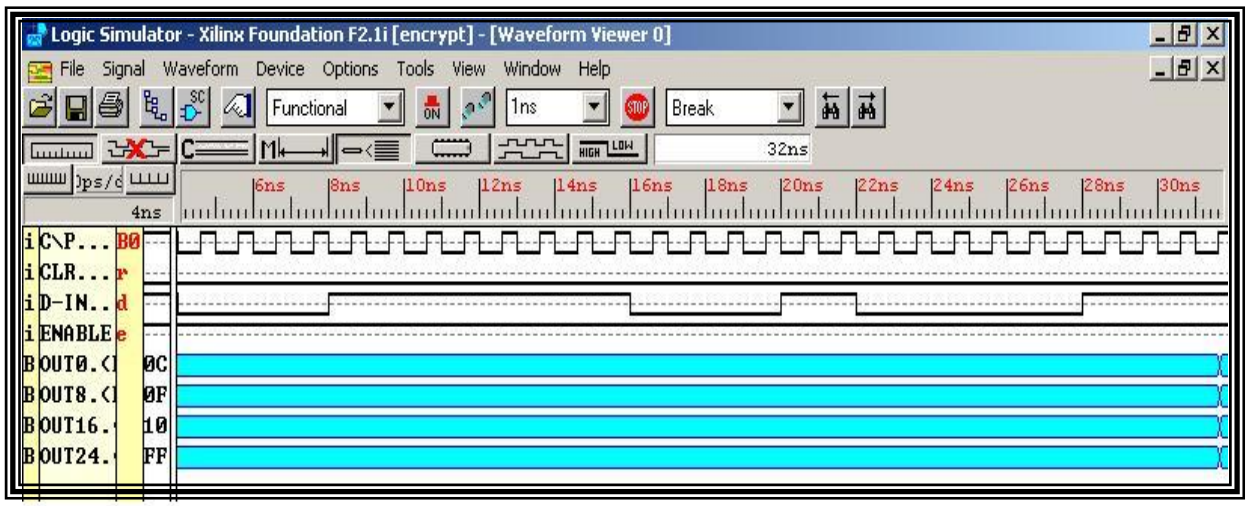

Fig (4): - Timing Diagram for the input and output data of the circuit

Table (1): - The transmitting system bit flow table

I/P	*Circuit Manipulating, Coding, and Scrambling*							*O/P*	
1111111	*Bit - Manipulation*	*11111111*	*FF*	*Processing*	*00010000*	*IO*	*Bit - Scrambling*	*11110000*	*FO*
0010000		*00010000*	*IO*		*11111111*	*FF*		*00110000*	*3O*
0001111		*00001111*	*OF*		*00001100*	*OC*		*11111111*	*FF*
0001100		*00001100*	*OC*		*00001111*	*OF*		*00001000*	*O8*

Table (2): - The receiving system bit flow table

I/O		*Circuit Manipulating, Coding, and Scrambling*						*O/P*	
11110000	*F0*	*Bit De-Scrambling*	*00010000*	*I0*	*Processing*	*11111111*	*FF*	*Bit - Manipulation*	*11111111*
00110000	*30*		*11111111*	*FF*		*00010000*	*I0*		*00100000*
11111111	*FF*		*00001100*	*0C*		*00001111*	*0F*		*00011111*
00001000	*08*		*00001111*	*0F*		*00001100*	*0C*		*00011000*

5. Conclusions

The aim of this paper is to propose a new circuit design for the implementation and evaluation of text coding systems using the FPGA platforms.

In this design the DSP point of view was adapted, where nearly in all other designs the implemented circuits is adapted from the communication point of view. This type of designs need no wide range of circuit design in which we reduces the cost. And because of the kit wide capabilities high speed, high accuracy, low cost, low power consumption, so the transmitting and receiving circuits may be implemented on the same platform.

Other privilege is achieved by overcoming the disadvantage of the conventional text coding systems that suffers from, where the data may appears byte by byte (serially) or they may appear in parallel form. This needs no large circuit to handle this task or it needs a global synchronization to keep system accuracy where any simple combinational circuit can handle the job properly.

With all what had mentioned above, the high speed circuit can handle several tasks at a time because in many applications the text size is not in need for very high speed circuits to be 1GHz operating frequency which leads to implement Several – In – One tasks. This will reduces the time, place, cost, power, and complexity.

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