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LOW COST REVERSIBLE SIGNED CONVERTER

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Abstract

The image compression required signed data that has a symmetric about zero to improve the efficiency of the compression. The unsigned images will convert to signed images using 1'complement (1'C) converter or 2'complement (2'C) converter.

The converter (1'C or 2'C) has two problems first is the transform is not reversible because the overlap in the last two values for 1'C or the first two values for 2'C. Second it is high cost for the general converter. The proposed method is a hybrid method between 1'C and 2'C make the overlap in the middle two values, that will give a reversible conversion and it has a very low cost for the general converter.

الخلاصة

إن معظم أنظمة ضغط الصورة تحتاج إلى بيانات ممثلة بطريقة حمل الإشارة في حين إن بعض الصور تخزن بطريقة المقدار فقط. لذا فان عملية ضغط الصورة تحتاج إلى تحويل البيانات الممثلة بطريقة المقدار فقط إلى بيانات ممثلة بطريقة حمل الإشارة.

إن هذه العملية تتطلب طرح مقدار مساوي لنصف القيمة القصوى. و تتم هذه العملية باستخدام المتمم الثنائي أو الأحادي الرقمي وكلتا الطريقتين تعد غير عكسية بسبب حصول تراكم في البيانات عند أول أو آخر قيمتين.

إن الطريقة المقترحة تستخدم المتمم الأحادي للنصف الأول من البيانات و المتمم الثنائي للنصف الثاني وهذا التهجين سيؤدي إلى حصول تراكم في البيانات عند القيمتين الوسطى و التي ستمثل صفر موجب و صفر سالب و هذه القيمتين تكون متساوية في المقدار عند إجراء الحسابات إلا أنها تعيد قيم مختلفة عند إعادتها إلى بيانات ممثلة بطريقة المقدار. إضافة إلى أن هذه الطريقة سوف تعطي دائرة رقمية ابسط بكثير من تلك التي تعطيها الطريقتين الأساسية.

Key Words

Signed converter, 1'complement, 2'complement, digital adder, adder/subtractor, FPGA, Xilinx, Virtex.

1- Introduction

The codec in the image compression systems expects its input sample data to have a nominal dynamic range that is approximately centered about zero. The preprocessing stage of the encoder simply ensures that this expectation is met. Suppose that a particular component

has **n-bits/sample**. The samples may be either signed or unsigned, leading to a nominal dynamic range of $[-2^{n-1}, 2^{n-1}]$ or $[0, 2^{n}-1]$ respectively. If the sample values are unsigned, the nominal dynamic range is clearly not centered about zero [1].

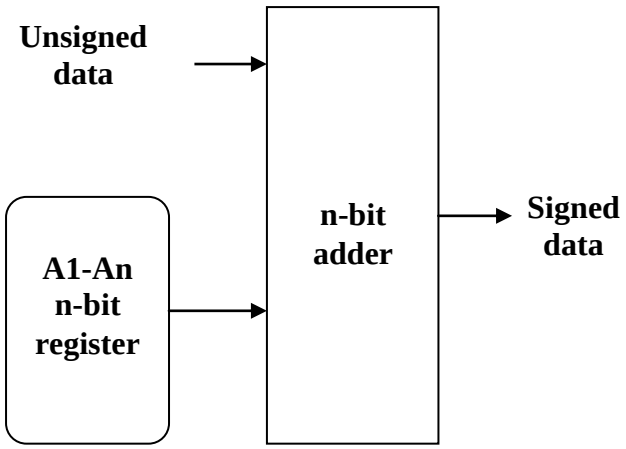
Thus, the nominal dynamic range of the samples is adjusted by subtracting a bias of 2^{n-1} from each of the sample values. If the sample values for a component are signed, the nominal dynamic range is already centered about zero, and no processing is required. By ensuring that the nominal dynamic range is centered about zero, a number of simplifying assumptions could be made in the design of the codec.

The post processing stage of the decoder in the image compression systems essentially undoes the effects of preprocessing in the encoder. If the sample values for components are unsigned, the original nominal dynamic range is restored. Lastly, in the case of lossy coding, clipping is performed to ensure that the sample values do not exceed the allowable range [2] .

2- Signed Converter

There are two types of the classic signed n-bit converter. First is the 2'C signed n-bit converter that is a circuit subtract a constant value that equal to [2^{n-1}] from the unsigned data. Second is the 1'C signed n-bit converter that is a circuit subtract a constant value that equal to [2^{n-1} -1] from the unsigned data. The general circuit of the two types is in **fig(1)** using n-bit register with n-bit adder/subtractor.

The classic signed n-bit converter can be implement-using FPGA that will give a high speed and low cost. The implementation of classic signed n-bit converter required 8–n cells with delay time equal to ng/2 sec where n is the number of bits in data bus and g is the delay of the basic cell of FPGA [3].



Fig(1): circuit of the classic signed n-bit converter

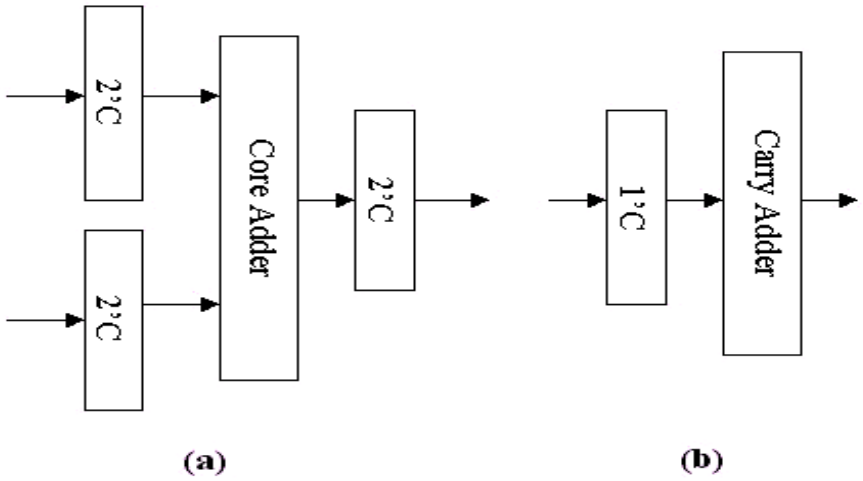
3- Adder/Subtractor Components [4,5,6]

There are two approaches to built adder/subtractor firstly by use the 2'complement as shown in fig(2), secondly by use the 1'complement as shown in fig(3).

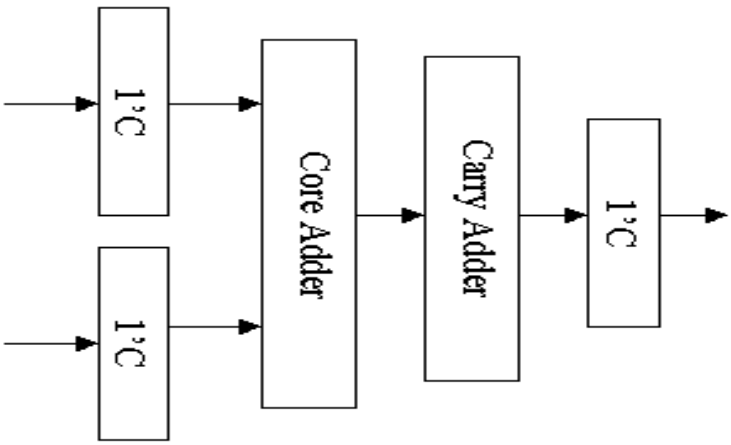
Table (1) shows the 1'complement method has same speed but it is lower cost from 2'compement because it need to one carry adder when 2'complement need to two carry adder outputs.

Table (1): The rational delay and cost of 1'C and 2'C Add/Sub.

Component	1'C Circuit	Carry Adder	2'C Circuit	Core Adder	1'C Add/Sub	2'C Add/Sub
Rational Delay	1	5	6	10	17	17
Rational Cost	1	10	11	20	33	44



Fig(2): Block diagram of 2'C adder/subtractor a) Total circuit b) 2'C circuit.



Fig(3): Block diagram of 1'C adder/subtractor.

4- The Proposed Method

The classic signed n-bit converter (1'C or 2'C) has two problems first is the transform is not reversible because the overlap in the last two values in 1'C or the first two values in 2'C. Second it is a high cost for the general converter when implemented using FPGA.

The idea of the proposed method is that use a 1'C for the values less than 2^{n-1} and 2'C for the values higher or equal to 2^{n-1}. This hybrid method between 1'C and 2'C make the overlap in the middle two values as in the following example in table(2) that represent the result of a signed 3-bit converter using the three methods.

The result in table (2) shows that the 1'C and the 2'C have two equivalent values that come from two different values. However, the proposed method give two equivalent values in magnitude but different in sign in the middle of the values (-0, +0). These two values will give a reversible conversion as shown in example in table (3) that represents the result of inverse of a signed 3-bit converter using the three methods.

Table (2): The result of a signed 3-bit converter.

Unsigned	**1'C**	**2'C**	**Proposed**
n2 n1 n0	**s n1 n0**	**s n1 n0**	**s n1 n0**
0 0 0	1 1 1	1 1 1	1 1 1
0 0 1	1 1 1	1 1 0	1 1 0
0 1 0	1 1 0	1 0 1	1 0 1
0 1 1	1 0 1	1 0 0	1 0 0
1 0 0	0 0 0	0 0 1	0 0 0
1 0 1	0 0 1	0 1 0	0 0 1
1 1 0	0 1 0	0 1 1	0 1 0
1 1 1	0 1 1	0 1 1	0 1 1

Table (3):The result of inverting of a signed 3-bit converter.

Original	**Inv. 1'C**	**Inv. 2'C**	**Inv. Proposed**
n2 n1 n0	**s n1 n0**	**s n1 n0**	**s n1 n0**
0 0 0	0 0 0	0 0 0	0 0 0
0 0 1	0 0 0	0 0 1	0 0 1
0 1 0	0 0 1	0 1 0	0 1 0
0 1 1	0 1 0	0 1 1	0 1 1
1 0 0	0 1 1	1 0 0	1 0 0
1 0 1	1 0 0	1 0 1	1 0 1
1 1 0	1 0 1	1 1 0	1 1 0
1 1 1	1 1 0	1 1 0	1 1 1

The result in table (3) shows that the result of the two classic methods of the signed/unsigned is not reversible, while the proposed method of the signed/unsigned is a reversible.

5- The Implementation of a General Signed N-Bit Converter

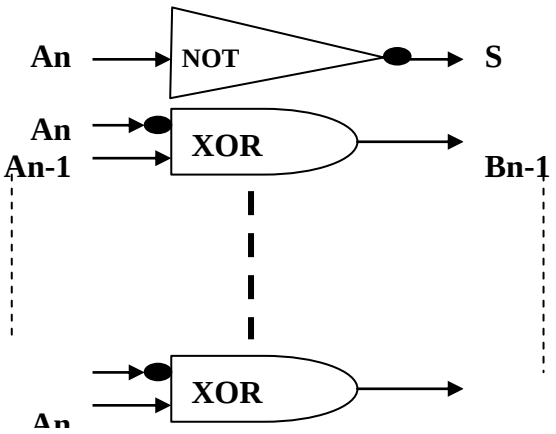
The implementation of the classic signed n-bit converter as shown in fig(1) requires to n cells for the n-bit register and 9n-2 cells for the adder/subtractor circuit, the total cost is 10n-2 with maximum delay equal to (2n+2)g sec.

The implementation of the proposed signed n-bit converter requires totally as shown in fig (4) to n cells with maximum delay equal to 1g sec.

6- Conclusions

The two classic methods of signed converter has an overflow in first two values in 2'C or last two values in 1'C. However, the proposed method is a hybrid method that will use the 2'C method for the first half of values and 1'C method for the last half of values.

This hybrid method wills have an overflow in middle two values, that will give a two advantages the first it is reversible because the two overlapped values have same value (0) with different pseudo sign (+0, -0). The second advantage it has a very simple circuit. This simplicity come from the two classic methods required to adder/subtractor while the proposed required to just XOR and NOT operations. The simple circuit will give a low cost circuit and very high speed because the direct implementation as shown in fig(4).



Fig(4): Digital circuit of the proposed signed n-bit converter.

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