Journal of Engineering and Development, Vol. 17, No.2, 2013, ISSN 1813- 7822

A Fully Integrated Traveling Wave Amplifier with 900 dBGHz Gain-Bandwidth Product

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Abstract:

In this paper, an integrated Traveling-Wave Amplifier (TWA) using Monolithic Microwave Integrated Circuit (MMIC) technology is proposed and carefully implemented. The classical structure of the five-stage amplifier is modified depending on the matrix form instead of the cascaded form with just one cell at each row of the matrix. This modification is shown to render the amplifier suitable for very large Gain-Bandwidth Product (GBP) operation in small on-chip area. Microwave office program simulation of the proposed design shows that it has excellent performance as compared to the conventional amplifiers with smaller area. The forward gain is 30dB with ±1dB flatness and 3dB bandwidth of about 30 GHz, which is the best results reported till now. The TWA is suitable for Digital Video Broadcasting (DVB) and satellite applications.

Keyword: Microelectronics, Traveling wave amplifier, MMIC.

مكبر الموجة المنتقلة المتكامل تماما 900 dBGHz حاصل ضرب كسب النطاق الترددي

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الخلاصة:

تم في هذا البحث اقتراح مضخم مرّحل الموجة ونُفِذت بدقة ضمن دائرة متكاملة باستخدام تكنولوجيا الدوائر المتكاملة المتآلفة للموجات الدقيقة. تم تحديث الهيكل التقليدي لهذا النوع من المضخمات وذلك بإعتماد تركيبة المصفوفة بدل تركيبة التسلسل مع استخدام خلية واحدة في كل صف من صفوف المصفوفة المتكونة من خمسة مقاطع. هذا التحديث يُزيد من عامل (الكسب ×عرض حزمة الترددات) و باستغلال مساحة اصغر على الدائرة المتكاملة. تم اختبار دائرة المضخم باستخدام البرنامج المتخصص (MWO) وكانت النتائج ممتازة

بالمقارنة من كل الدوائر المصممة سابقا. إن الربح الأمامي يساوي 30dB مع تسطح بمقدار ±1dB و عرض نطاق يساوي 3dB لـ 30 GHz وهذه احسن نتائج منشوره لحد الان. ان المضخم المُرّحل للموجة ملائم لتطبيقات الاقمار الصناعية و البث الفديوي الرقمي.

1. Introduction:

Traveling **W**ave **A**mplifier or TWA is a technique which achieves extremely broadband operation with very low noise, shown in Figure.1 [1]. The idea behind it is that, instead of trying to tune out the transistor parasitic capacitances, these capacitances are used as part of a lumped-element transmission line. On the input side, inductors L_g are placed between the gate-to-source capacitances C_{gs} of the adjacent transistors, and in that way the familiar lumped-element artificial transmission line with a characteristic impedance of $Z_g = L_g / C_{gs}$ is formed. This transmission line can be resistively terminated at the end with little loss of input signal. On the output side, inductors L_d are placed between drain-to-source capacitances C_{ds} of the adjacent devices, and a transmission line with a characteristic impedance $Z_d = L_d / C_{ds}$. This is an active transmission line and the signal builds up along it. The phases of the outputs of the individual transistors will only be appropriate for left-to-right propagation, so little power will be lost in the resistive termination at the left end of the line. In effect, the two transmission lines are coupled lines with a coupling coefficient greater than unity. The inductors L_g and L_d can be chosen to equalize the characteristic impedances between the cells of the input and the output lines.

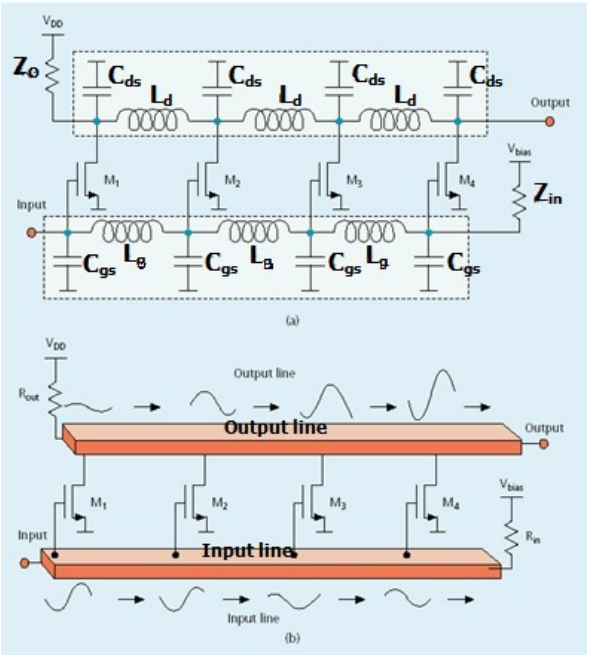

Figure.1 General Structure of a 4-cells TWA

These characteristic impedances must be equal to the matching impedances $\mathbf{Z_{in}}$ and $\mathbf{Z_o}$ in order to minimize the reflection losses at the input and output ports ($\mathbf{S_{11}}$ & $\mathbf{S_{22}}$). The input signal Vin travels down the gate line to the terminated end $\boldsymbol{Z_g}$, where it is absorbed. As the signal travels down the line, it will be amplified at each stage and transferred to the drain line through the transconductance ($\boldsymbol{g_m}$) of the transistors. The signals on the drain line add in the forward direction as they arrive at the output. The power gain equation for a lossless amplifier is given by [1]:

$$G = \frac{g_m^2 Z_d Z_g N^2}{4} \quad \text{.....(1)}$$

where N is the number of sections or cells.

The bandwidth of the amplifier is determined by the cutoff frequency of the **L-C** ladder circuit of the transmission lines. If $\boldsymbol{L_g = L_d = L}$, **and** $\boldsymbol{C_{gs} = C_{ds} = C}$, **then :**

$$\omega_c = \frac{2}{\sqrt{LC}} \quad \text{.. .....(2)}$$

Prior to 1960, nearly all microwave equipments utilized Microwave Discrete Circuits (**MDCs**), which are made of separate elements connected together by conducting wires. Since the trend of developing electrical technology is toward smaller size, lighter weight, lower cost, and increased complexity and reliability,

microwave technology has been moving in this direction for the last thirty years with the great progress in monolithic microwave integrated circuit (**MMIC**) design [2]**.** In MMIC all active and passive elements or components are grown on a substrate surface. The substrate must be a semiconductor material in order to enable the fabrication of the active devices. The type of the devices and the operating frequency range dictate the material of the substrate. However discrete circuits are still very useful in high-power microwave systems. The integrated circuit technology serves to replace bulky and expensive discrete components and coaxial lines with small and inexpensive planar transmission lines and components which can be integrated on a chip that is only a few square millimeters in size. The geometric representation of the components and interconnections within the integrated circuit is known as circuit "layout". The main drawback associated with the design of the **MMIC** is the effect of the parasitic elements **(R-L-C**) which appear with each component in the circuit. These parasites skew the performance of the circuit, so optimization methods have to be used to achieve optimal design.

2. Historical Review:

In more recent years, several TWAs for microwave application were reported. Most of them are based on **Si** CMOS technology because of the advantages of low cost and integration ability with baseband circuits. The performances of these amplifiers are shown in **table.1** below. In 2002 a TWA using 4-stages in the basic form was fabricated in a 0.18µm CMOS process with 8dB ±1.5dB gain form 0-to-l0 GHz [3]. Another one was presented in 2004 in a 0.12µm SOI CMOS technology with 9 dB gain and ±1dB ripple in the frequency range 5-86 GHz using 7-stages structure [4]. In 2005 three 6-stages CMOS TWAs were proposed: 9.5 ±2dB gain with bandwidth of 32 GHz [5], 9.7 ±1.6dB gain with ≈50 GHz bandwidth [6], and 7.4 ±1dB gain with ≈80 GHz bandwidth [7]**.** A broadband amplifier employing cascaded single-stage was designed and fabricated in 2010 using a discrete circuit with three different DPHEMT devices in the three respective stages of the design to further enhance the amplifier's performance. The amplifier achieved an associated gain level above 25 dB with flatness of ±1 dB across 2–18 GHz. The big size of this circuit was because of the use of discrete technology in stead of the IC [8]

Table.1 Comparison of different TWAs

Technology	BW (GHz)	Gain (dB)	No. of stages	Flatness (dB)	Chip Area (mm^2)	GBP (dB×GHz)	Ref.
0.18µm CMOS	1-10	8	4	±1.5	1.3×1.8	72	[3]
0.12µm SOI CMOS	5-86	9	7	±1	1.46×0.72	729	[4]
0.18µm CMOS	0-32	9.5	6	±2	0.94×0.86	304	[5]
90nm SOI CMOS	10-59	9.7	6	±1.6	0.3×1	475	[6]
90nm SOI CMOS	0-80	7.4	6	±1	-	592	[7]
DPHEMT	2-18	25	3	±1	5×6	400	[8]

The operating gain-bandwidth products of the previously published TWAs are all below than 729 dBGHz. In this paper, the highest GBP is wanted to be reported in a traveling wave amplifier using a standard SOI CMOS.

3. Matrix Amplifier:

Since the gain of TWAs depends on the number of stages or cells according to **equation (1),** then, to achieve higher gain, more stages should be cascaded, which means increasing the size of the amplifier and increasing the parasitic elements in the circuit which affects the overall performance . A better solution was proposed by Niclas and Pereira in [9]**.** The amplifiers are stacked with the gate line of the latter amplifier overlapped by the drain line of the former one. Then, a combination of additive and multiplicative amplification occurs in one module without bandwidth reduction. The new module is very much similar to the M × N rectangular matrix, where M is the number of tiers or rows and N is the number of sections in each row. To optimize the matrix amplifier, just one stage will be used in each row of the amplifier by which, the multiplicative gain will be achieved in stead of the additive gain of the classical TWAs. The available power gain expression is given by:

$$G = \frac{g_m^{2N} Z_g^{2(N-1)} Z_d^2}{4} \qquad \text{.....(3)}$$

Comparison of equations **(1)** and **(3)** shows that higher gain can be realized from optimized matrix amplifier configuration. This is because its gain is an exponential

function of the stage's number, whereas the gain of the conventional TWA is only proportional to the square of the number of stages.

4. Implementation of on-Chip Circuits:

A few years ago, the world of monolithic microwave ICs returned to silicon semiconductor to provide lower cost solution in the commercial market. It exhibits suitable physical properties for the fabrication of active devices [10]. Also, it can be easily oxidized to form SiO_2, which is useful for constructing capacitors and MOSFETs. The relative permittivity (or dielectric constant) of the silicon semiconductor is 11.7

The MOSFET is used to achieve the active device of the amplifier because of its low power consumption and small on chip area occupation of the CMOS devices which lead to the Very Llarge Scale Iintegration (VLSI) capability. The physical structure of N-MOSFET is shown in **Figure.2**. In this figure, *L* and *W* are the dimensions of the gate region; t_{ox} is the thickness of silicon dioxide (SiO_2) layer, which covers the area underneath the gate region, (therefore the MOSFET is also named insulated-gate FET or IGFET). **Figure.3** shows an approximated small-signal equivalent circuit for the transistor showing the important parasitic elements.

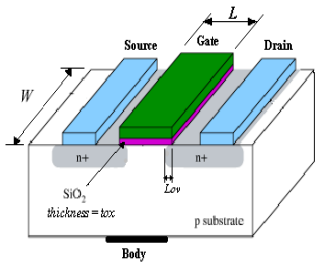

Figure.2 Physical structure NMOS transistor

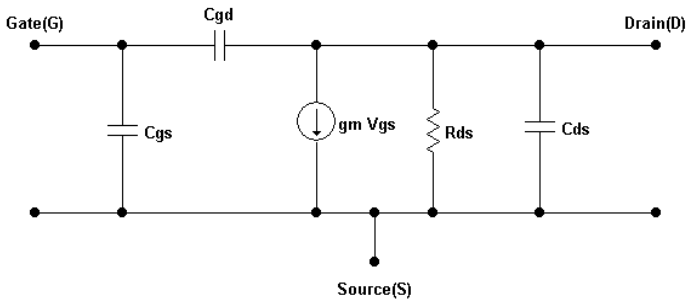

Figure.3 High frequency model of the transistor

One of the important characteristics of NMOS transistor in the design of the amplifiers is the transconductance (g_m) which is given by [11]:

$$g_m = \mu_n C_{ox} \left(\frac{W}{L} \right) V_{ov} \quad \text{.....(4)}$$

where μ_n = the mobility of electrons in the channel (m^2/V.sec).

C_{ox} = the oxide capacitance (F/m^2).

W/L = the aspect ratio of the transistor.

V_{ov} = the overdrive voltage at which the transistor is operating (it is usually selected to be 0.2-3volt).

The other important characteristics are the parasitic capacitances. From **Figure.3** three capacitances can be identified, gate-source capacitance (C_{gs}), gate-drain capacitance (C_{gd}), and drain-source capacitance (C_{ds}). The value C_{ds} can be calculated using the dimensions of the drain plane and the substrate height. The two other capacitances can be found as:

$$C_{gs} = \frac{2}{3} W L C_{ox} \quad \text{.....(5)}$$

$$C_{gd} = W L_{ov} C_{ox} \quad \text{.....(6)}$$

where L_{ov} is the overlap area length which is typically about 0.05 to 0.1L.

Resistor's layout can be realized in planar form using thin film of resistive material placed on top of the oxide layer as shown in **Figure.4** . The resistance value of planar resistor is expressed as [11]:

$$R = \frac{\rho}{t} \frac{\lambda}{w_R} = R_s \frac{\lambda}{w_R} \quad \text{.....(7)}$$

where λ and w_R are the length and width of the resistive film respectively, ρ is the resistivity of the film (Ω.m), and t is its thickness. Note that ρ/t is the resistance per unit square (Ω/□). It is called the sheet resistance (R_s). The resistor area should be chosen as small as possible in order to minimize the values of parasitic components.

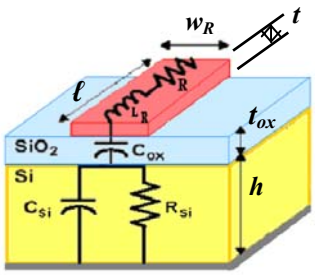

Figure.4 Layout of a planar resistor with the parasitic components

Planar capacitor in CMOS process is realized by any two parallel plates of conductors separated by the oxide layer as shown in **Figure.5**. The capacitance value can roughly be calculated using the following formula [11]**:**

$$C = \varepsilon_o \ \varepsilon_r \frac{A}{h_c} \qquad \text{…….(8)}$$

where ε_o is the permittivity of free space (8.854×10^{-12} F/m), ε_r is the relative permittivity of the insulator separating the metals (3.9 for S_iO_2) , A is the area of the metal, and h_c is the distance between the two metals.

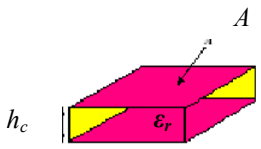

Figure.5 CMOS capacitor

The main problem associated with the design of microwave integrated circuits, in which the inductors are essential elements, is the physical size of these elements.

Both resistors and capacitors are easy to implement. Considerable effort has gone into the design of the inductor implementation. **Figure.6** shows the layout for a spiral inductors, and **Figure.7** is its model. For a given shape, an inductor is completely specified by the number of turns (n), the turn width (w), the turn spacing (s), and the turn diameters: d_{in} and d_{out} , where $d_{avg} = 0.5(d_{in} + d_{out})$. There are many expressions for the inductance value; one of them is given by a monomial expression that has the following form [12]:

$$L = \beta d_{out}^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5} \quad \text{.....(9)}$$

where $\beta = 1.62\times10^{-3}$, $\alpha_1 = 1.21$, $\alpha_2 = -0.147$, $\alpha_3 = 2.4$, $\alpha_4 = 1.78$, and $\alpha_5 = -0.03$.

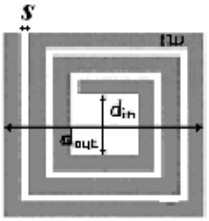

Figure.6 On chip inductor

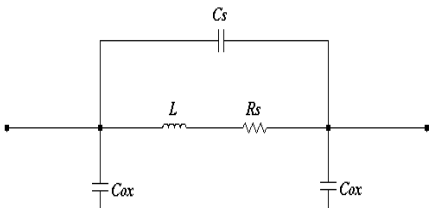

Figure.7 Spiral inductor model

In the electrical model of the passive elements, $\boldsymbol{R_s}$ is the conductor resistance, $\boldsymbol{C_s}$ is the series capacitance which appears between the turns of the inductor, $\boldsymbol{C_{ox}}$ is the capacitance in the oxide layer**,** $\boldsymbol{C_{si}}$ is the capacitance in the silicon substrate, and $\boldsymbol{R_{si}}$ is the resistive loss of the substrate.

Transmission lines (**TL**) are other important parts of microwave systems on which the signals travel between elements of the circuits. Microstrip line (MS) as illustrated in Figure.8, consists of two parallel conductors. The top conductor is a strip of metal formed on the oxide layer and used as the signal line. The bottom conductor

w_L

is the ground plane. Mounting of passive and active devices in series configuration is very easy with the use of microstrip lines.

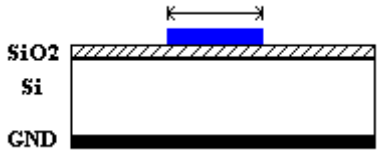

Figure.8 Microstrip transmission line

5. Proposed TWA:

The design procedures discussed in 3 and 4 are utilized in the practical design of a 5-stages ultra-wideband traveling wave amplifiers based on CMOS technology using coplanar strip transmission lines. The circuit layout of the amplifier is shown in **Figure.9.** The choice of transmission line width is a compromise between reducing the parasitic capacitance and increasing parasitic resistance and inductance. The thickness, height, and width of all transmission lines used in the work are: 4μm, 100μm, 10μm respectively. The separation between the inductors should be large enough to avoid electromagnetic coupling effects. All inductors in the circuit are formed in square spiral form with 10μm line width, 4μm line spacing, and 1.5 turns. On the other hand, the resistances of the circuit are in the sheet form with 10μm width, and 50 Ω/□ sheet resistance. It is clear that all the elements of the circuit need to be designed with the same width (10μm) in order to avoid the discontinuities and their parasites. In order to reach the target specifications, the circuit performance is optimized by tuning some of the component layout to compensate for the effects of the parasites.

The simulated results of the final circuit layout of the amplifier through Microwave Office program are shown in **Figures 10** and **11**. The measurements include the S-parameters as well as the stability factors (μ_s and μ_L). The forward gain (S_{21}) is 30dB with ±1dB flatness and 3dB bandwidth of about 30 GHz, which is the best results reported till now. The return losses (S_{11}) and (S_{22}) below -5dB over the entire bandwidth. The stability measures shows that the amplifier is unconditionally stable since $\mu_L, \mu_S > 1$ at all frequencies within the bandwidth range.

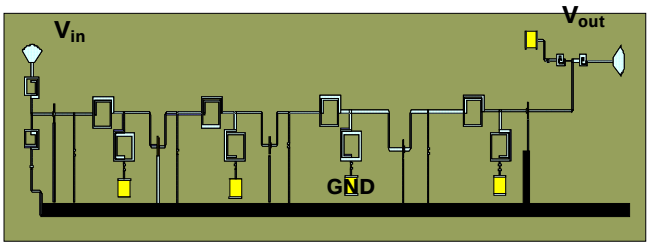

Figure.9 Layout of the proposed TWA

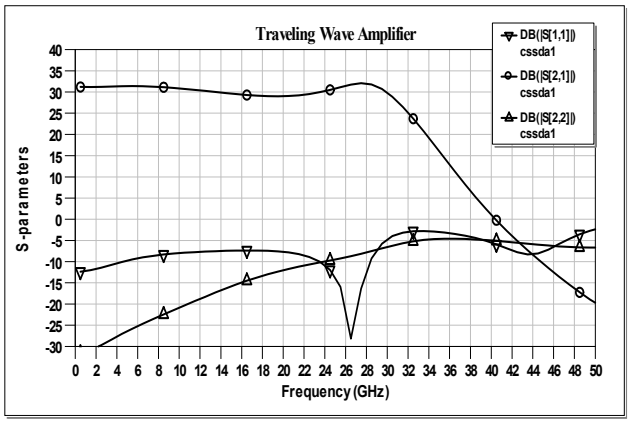

Figure.10 Measured S-parameters of the proposed TWA

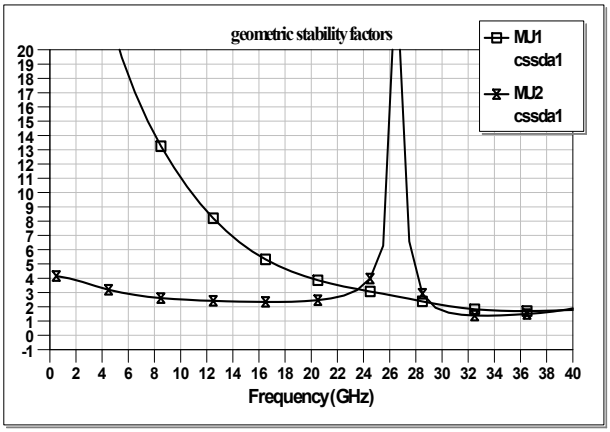

Figure.11 Measured stability factors of the proposed TWA

6. Conclusion:

Taking advantages of the matrix amplifier, a high-gain broadband TWA has been successfully designed and implemented using Si CMOS technology. The complete schematic and layout design were presented, and then tested. Simulation

results show that the amplifier provides 900dBGHz gain-bandwidth product with ±1dB flatness. The circuit occupies 4.6×1mm^2 area. The amplifier offers the best performance in CMOS technology in terms of high gain-bandwidth product, reduced circuit elements, and good gain flatness to this date to the author's knowledge.

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